Testing Times

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1 Testing Time for One Chip.

We measure the time to run the current tests on a single chip to be 3 min 35 sec, or 215 sec. This seems to be significantly different than the time reported by SCIPP group [1]. The latter time of about 2 min 30 sec is more consistent with the wafer testing time of about 11 hours, assuming that very small number of chips fails the initial DEAD/ALIVE test. The cause of the difference is not known yet. It might have something to do with different computer speeds.

We investigated the testing time breakdown with the setup we have. Most of the time is spent on the scan to determine gain, offset and noise, on the scan to measure the trim dacs parameters and on the running the test vectors, as shown in Table 1. The test vectors time dominates.

Table 1: Testing time breakdown by the test type.

Test Type	Time (sec)
Scan (gain, ...)	27
Trim DACs	31
Test Vectors	152
Others (Scan DACs, Power Consumption, Strobe Delay)	5
Total	215

1.1 The Test Vectors

The time to run the test vectors depends on the total length of all test vectors, on the number of times we run them, $\mathrm{N_{tv}}$, on the number of steps in Vdd, $\mathrm{N_{Vdd}}$, and on the number of steps in Frequency, $\mathrm{N_{Freq}}$. It is reasonable to expect the time to be proportional to $\mathrm{N_{Freq}} \times \mathrm{N_{Vdd}}$. As to $\mathrm{N_{tv}}$, with the current set of vectors, when looping over 9 Vdd values and 9 Frequency values, the total time depends on it linearly:

$$Time(sec) = 37 + 1.15N_{tv}$$

For $\mathrm{N_{tv}} = 100$ (this is the current default), we get 152 sec, for $\mathrm{N_{tv}} = 10$ the time is 49 sec. Clearly, we might want to reduce $\mathrm{N_{tv}}$, since we require the test vectors to be 100% efficient for the good chips [2].

One can notice that there is a rather large "idle" time of 37 sec even if we do not run the test vectors. The breakdown of this time is listed in Table 2. There still are some sleep statements. Saving the data on disk takes a relatively large time.

Table 2: TV idle time breakdown.

Process	Time (sec)	Comment
Current measurements	7	To stabilize the conditions before running a TV
Sleep statements	8	IMHO unnecessary
TV loading into VME board	9	Irreducible
Write data to disk	11	
Display Freq, Vdd	2	

1.2 Trim DAC Parameters

This time depends on the number of events per analog point, N_{an} in the following way:

$$Time(sec) = 11 + 4 \times (N_{an}/100)$$

The pattern of trim DAC points is preset (hardcoded) in software.

It takes 7 seconds to save these data to disk with the default value $N_{an} = 500$.

1.3 Scan for Gains etc

This time depends on N_{an}, on the number of steps in a threshold scan, N_{th}, and on the number of scans performed with different injected charges, N_{ch}:

$$Time(sec) = 1 + (N_{ch} \times N_{th}/100)(1.80 + 1.15 \times N_{an}/100)$$

It takes 4 seconds to save these data to disk with the default value $N_{an} = 500$.

If we change N_{an} from its current value of 500 to 100 and preserve all other parameters, then the time for this test reduces from 24 sec to 10 sec.

2 Conclusions

We can deduce the following conclusions:

- The testing time for a good chip is mostly spent on two analog scans and the test vectors.
- We verified that the testing time depends linearly on the number of events for both the test vectors and the analog tests. In this dependence, there is a substantial "offset" related to the test setup, saving the data to disk and other activities.
- There seems to be a substantial difference between the testing times for different setups. The cause is not known yet.
- If we can afford to reduce the N_{tv} to 10 and N_{av} to 100 [3], then the testing time for our set up would be 80 sec/chip, or less than 6 hours per wafer. This would indicate even shorter time for the SCIPP setup.

References

[1] Max Wilder, private communications.

[2] Carlos Lacasta, private communications.

[3] Tomorrow note on the relation between the testing parameters and precision, by Christian Flacco.