Testing I/O Signal Levels, Phases and Duty Cycles with LAST[1]

(*A Preliminary Description*)

Version 1.0
June 12, 2001
C. Vu, V. Fadeyev

[1] **LAST** stands for "**L**BNL **AS**IC **T**ester", aka "LBL Tester" or "new system".

Introduction

There is a short description of these tests in the ABCD Test Specifications (with better illustrated pictures). The intention of this note is to provide more details about the implementation, to allow other people to understand the methods and procedures involved, and to ease the software implementation.

The working ranges mentioned in this note are lifted from the Francis's notes in "ABCD Specification". As such, they are preliminary. Statistically large testing experience is required to set the final numbers.

I/O Signals and Test Vectors

We test the chip signal levels and phases by running test vectors (TVs) utilizing these signals and varying the conditions. The working range is exceeded when the test vector efficiency is below 100%. Care is taken to minimize signal interference, by employing TVs with isolated signal usage (Table 1). The additional TVs developed for these tests are:

- TEST DAT0 (simple pattern injection for a slave chip),
- TEST DAT1 (simple pattern injection for a slave chip),
- TEST #0 (chip as MASTER & END, do soft reset and trigger, look for the datalink/LED only),
- TEST TOK0 (chip as MASTER & MIDDLE, do soft reset and trigger, look for TOKENOUT0 only),
- TEST TOK1 (chip as MASTER & MIDDLE, do soft reset and trigger, look for TOKENOUT1 only).

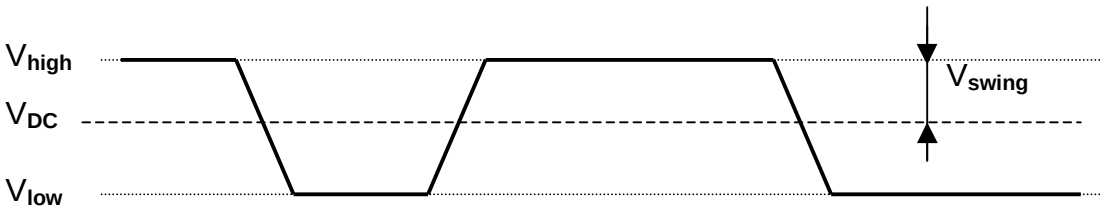
We should probably plan on doing each test twice, once at 40 MHz, and another time at higher frequency.

Table 1 I/O signals and the test vectors used to validate their properties.

Signal Name	Signal Type	Test Vector Used	TV Toggling Input Lines	TV Toggling Output Lines
CLK0	input	TEST #1	COM0	datalink/LED
CLK1	input	sibling of TEST #1	COM1	datalink/LED
COM0	input	TEST #1	COM0	datalink/LED
COM1	input	sibling of TEST #1	COM1	datalink/LED
DATAIN0	input	TEST DAT0	COM0, DATAIN0	DATAOUT0
DATAIN1	input	TEST DAT1	COM0, DATAIN1	DATAOUT1
TOKENIN0	input	TEST #5, also with delayed TOKEN	All	All
TOKENIN1	input	TEST #5, also with delayed TOKEN	All	All
datalink/LED	output	TEST #0	COM0	datalink/LED
DATAOUT0	output	TEST DAT0	COM0, DATAIN0	DATAOUT0
DATAOUT1	output	TEST DAT1	COM0, DATAIN1	DATAOUT1
TOKENOUT0	output	TEST TOK0	COM0	datalink/LED, TOKENOUT0
TOKENOUT1	output	TEST TOK1	COM1	datalink/LED, TOKENOUT1

Input Levels

The ABCD input differential signals are provided by the pin driver chips, which are housed by the connector board in the blue box. Two chips are supplied for each signal, e.g. one for COM1 and one for COM1B sides of the COM1 input. Each pin driver chip has two input voltages, set by DACs, which define the high and low voltage levels for the output signal (and correspondingly, the ABCD input signal swing).



To do the test for an input signal, we set all other signals at nominal conditions and scan the input swing by changing the pin drivers input voltages supplied by DACs. We run a test vector, for which the signal changes its state multiple times. The voltage values, for which the test vector is 100% efficient, define the signal working range for the chip being tested.

The upper scan limit of the swing is defined by the signal DC level, V_{DC}, since the lower output voltage level $V_{low} = V_{DC} - V_{swing}$ has to be positive (DACs cannot provide a negative voltage). The limit is 1.2 V for the datalink/LED and 2.0 V for all other signals.

The lower scan limit is defined by the hardware capabilities. The pin driver chips cannot provide a near-zero voltage difference on the output. The signal shape is distorted at the beginning of a pulse below dV of about 160-200 mV. The distortions may not be an issue, since the ABCD input clock is shifted with respect to other signals by half a clock cycle. The minimal dV one can set is 65 mV.

The histogram of the test vector efficiency as a functions of the voltage swing is stored in the data files. The offline data analysis algorithm should find a minimal value of the swing $minV_{swing}$ at which the chips is working. The cut on minVsw should probably be placed near the specified maximum value (Table 2).
An example plots are shown in Figure 1.

Table 2 Input signal levels range and selection.

Signal Name	Specified Working Range	Selection Cut on $minV_{swing}$
CLK0	V_{swing} **< 100** mV	?
CLK1	V_{swing} **< 100** mV	?
COM0	V_{swing} **< 100** mV	?
COM1	V_{swing} **< 100** mV	?
DATAIN0	[40, 160 mV]	160 mV
DATAIN1	[40, 160 mV]	160 mV
TOKENIN0	[40, 160 mV]	160 mV
TOKENIN1	[40, 160 mV]	160 mV

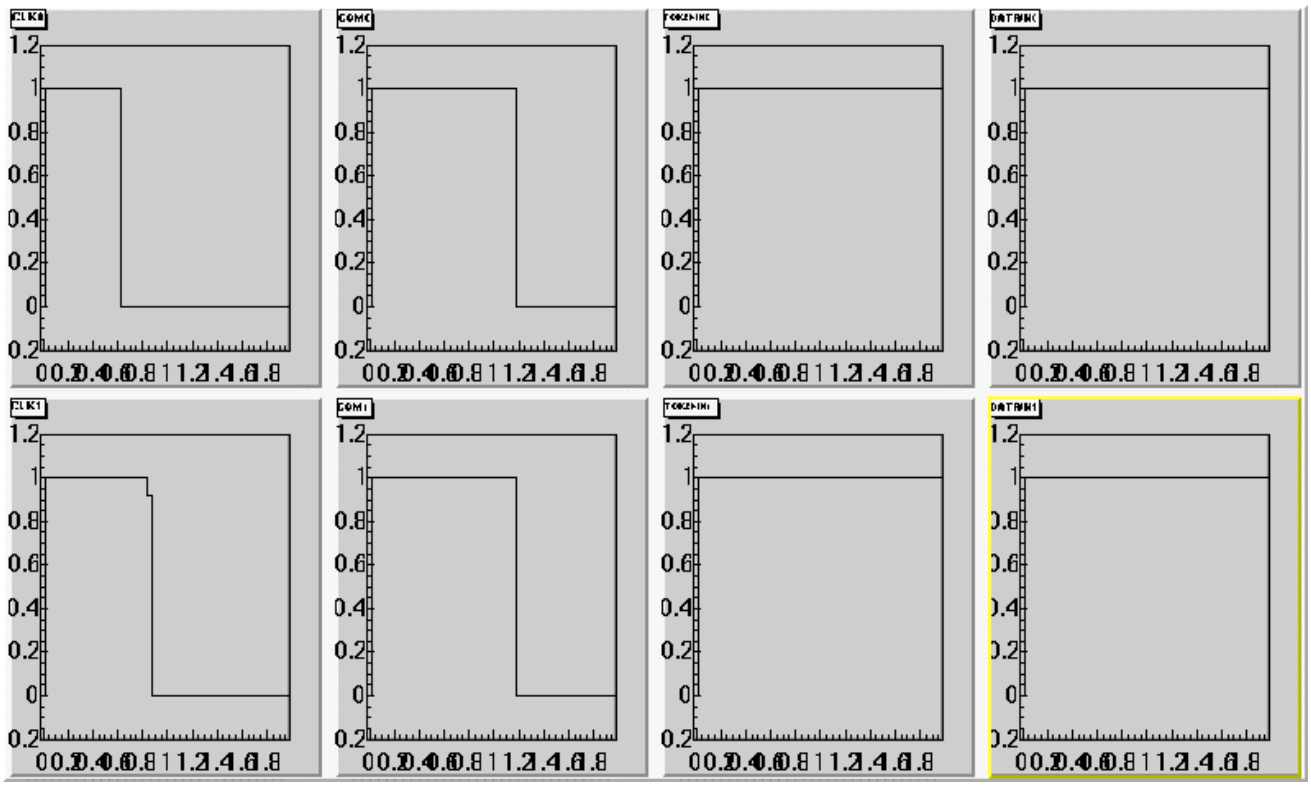


Figure 1 Input signal levels scan. Test Vector efficiency is shown as a function of the signal swing (in V) for each input differential signal.

Output Signal Levels

Each differential output signal of the ABCD goes through a differential amplifier (DAMP) and a window comparator (WC). The DAMP amplification factor is 3. More information about the scheme is available in the System Description writeup. A signal passes through the corresponding window comparator if its high level is above the WC thresholds and its lower level is below the WC thresholds.

To test the levels of a signal, we run a test vector which toggles its value and scan the WC thresholds, with both thresholds set to the same value. We expect that the TV efficiency would have a plateau centered at the differential amplifier voltage level (1.2V for datalink/LED and 2.0V for all other signals). The test vector efficiency transitions between 100% and 0% efficiency indicate the high and low signal voltage levels.

The allowed scan range is between 0 and 4V. The precision is set by the 10 bit DACs and the resistors in the DAMP circuit (about 1%).

The data are stored as the efficiency histograms. The offline analysis should identify the transitions and find the voltage swing (half the difference between the transitions region divided by the factor of 3). It would be good to also find the center of the plateau region, to see if it coincides with the reference voltage. A significant difference found for all chips on a wafer would indicate hardware problems. If a difference is found for one chip only, then that chip's output driver(s) might be bad.

The example plots for the output signals are shown in Figure 2.

Table 3 Output signals swing specifications.

Signal Name	Specified Working Range for V_{swing}
datalink/LED	[250, 400 mV]
DATAOUT0	[40, 160 mV]
DATAOUT1	[40, 160 mV]
TOKENOUT0	[40, 160 mV]
TOKENOUT1	[40, 160 mV]

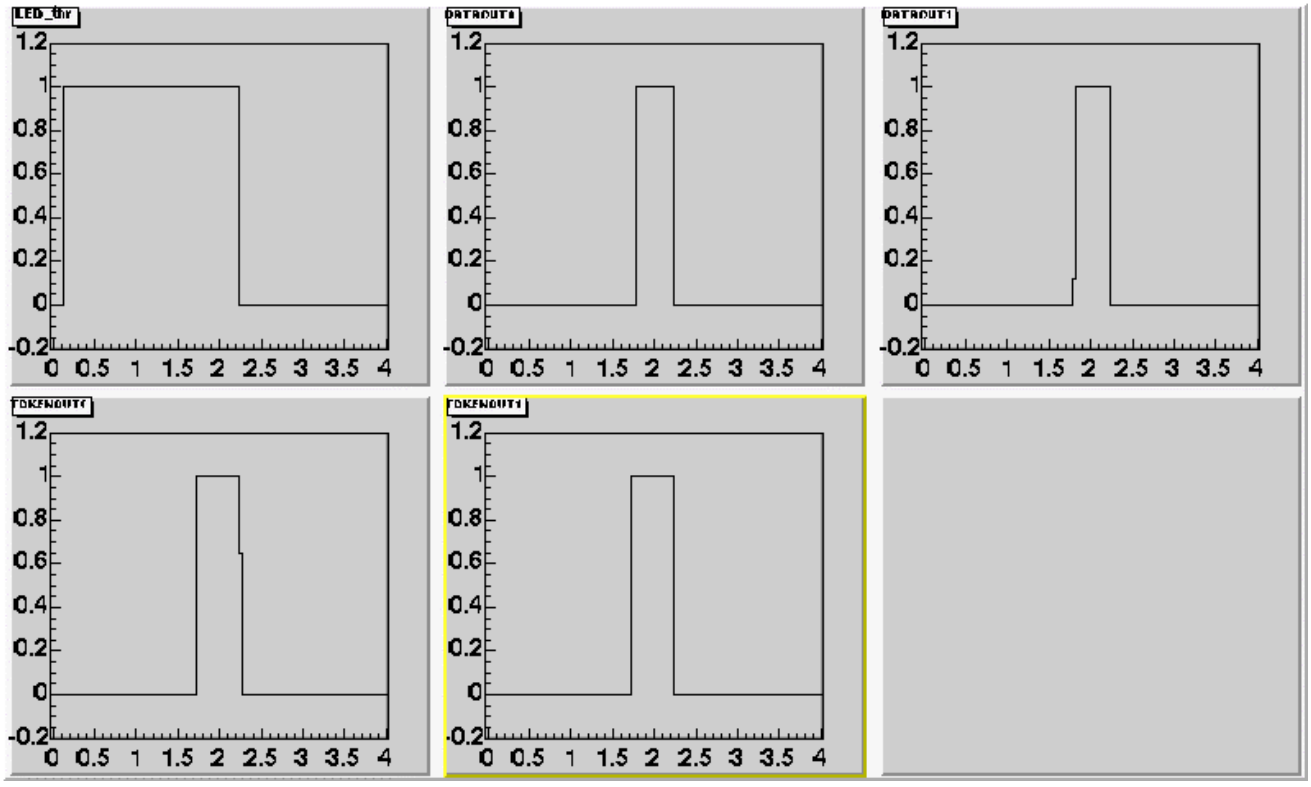


Figure 2 ABCD Output signal levels scans, the test vector efficiency as a function of the window comparators thresholds. The thresholds are scanned between 0 and 4 V.

Input Signals Phases

Each of the input signals passes through a delay chip, therefore there is a capability to scan its phase wrt clock. The total scan range is about 30 ns, the minimal step size is about 0.06 ns.

For each signal, the delay is scanned while other signals (including clocks) are kept at nominal conditions. To cover the full scan range, we do two scans for TOKENIN signals, one is with the "usual" version of the test vector #5, and another with the simulation file assuming that the TOKENIN signal is delayed by 1 clock cycle. This is due to the fact that the TEST #5 changes the state of all input and output signals, therefore their relative timing matters. The TVs used for the COM and DATAIN signals are such that only one output signal varies (either datalink/LED or DATAOUT), and the shift of the entire chip response by 1 clock cycle does not affect the comparison.

The test vector efficiency is 0% when the signal is in phase with the clock inside the chip. It rises to 100% immediately afterwards. There can be a sizable region of zero efficiency before the "in phase" condition, which is due to the setup time.

When a signal and the corresponding clock are in phase inside the chip, their actual delays set in hardware may be different, due to different signal propagation times in the input circuits. The input differential signals can be classified into two groups:

- CLK and COM signals,
- DATAIN and TOKENIN.

The propagation time is expected to be similar for signals within each group. It can be rather different for the two groups (we observed a difference of about 6 ns before).

The data are stored as the histograms of the test vector efficiency as a function of the time delay. The offline analysis should identify:

- the propagation time difference (called "Phase Delay" in Table 4) between a signal and a clock by the 0% -> 100% efficiency transition,
- the signal setup time, as the width of sub-100% efficiency dip.

An example histogram is given in Figure 3.

Table 4 Input signal phases specifications.

Signal Name	Setup Time Range, ns	Phase Delay, ns
COM0	[9,20]	?
COM1	[9,20]	?
DATAIN0	[0,15]	?
DATAIN1	[0,15]	?
TOKENIN0	[0, 9]	?
TOKENIN1	[0, 9]	?

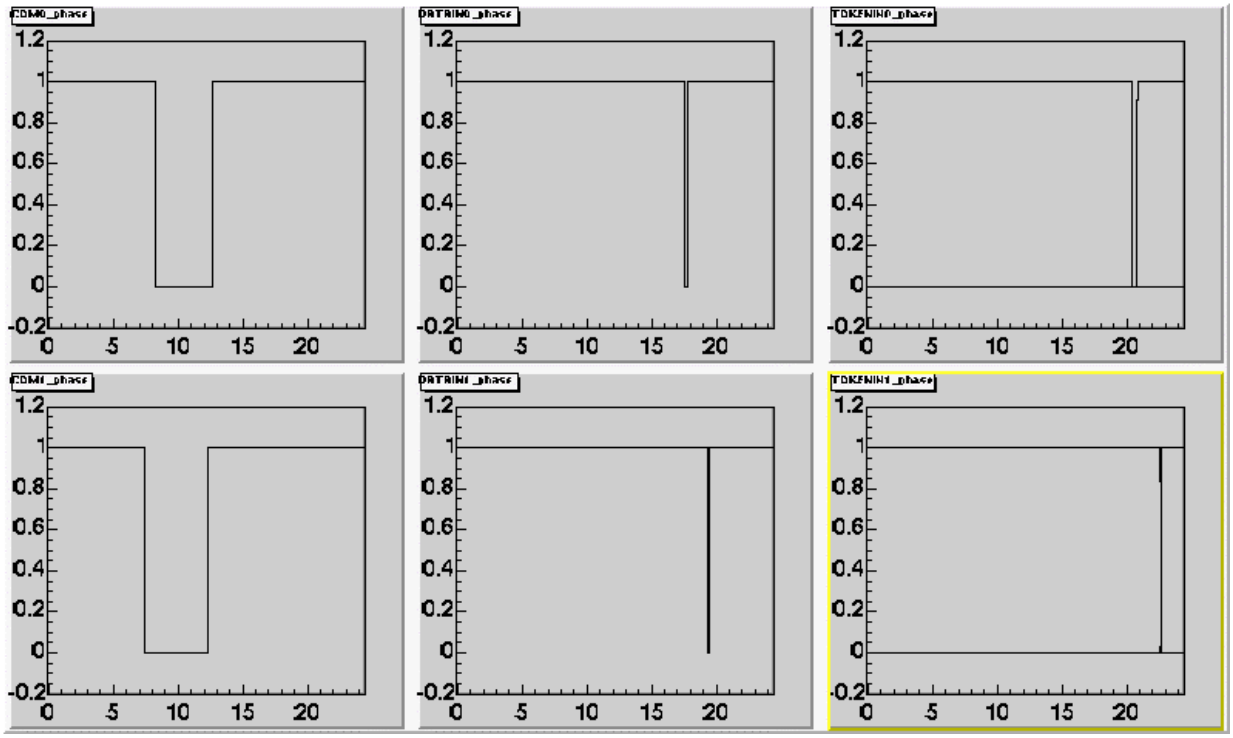


Figure 3 The scan of the input signal phases. The test vector efficiency is shown as a function of time delay (in ns). Two curves are plotted for the TOKENIN signals, one is for the "usual" TEST #5, and one for the version with TOKENIN signal delayed by 1 clock cycle.

Output Signals Phases

All the output signals are passed through a register. The latching clock for this register can be delayed. The delay range is the same as for the input signals delays. This feature is used to find the phase of an output signal relative to the clock. When the phase is zero, there is an efficiency loss for the test vector.

When running a test vector for a given signal, other output signals are masked off in the data vs. simulation comparison to avoid interference (which may result in multiple dips in the efficiency histogram). For datalink/LED and DATAOUT signal we use the test vectors which does not have other output lines toggling. For TOKENOUT signals we use test vectors which have both datalink/LED and TOKENOUT lines toggling, although only TOKENOUT is being enabled. Therefore, two efficiency dips may occur in this case. The position of one of them is known from the datalink/LED phase measurement.
The data are stored as the efficiency histograms. The offline analysis should identify the position of the efficiency dips. For the TOKENOUT signals, two dips may occure, and the right one should be chosen (the position of the wrong one is the same as for the datalink/LED signal).

Table 5 Output signals phase specifications.

Signal Name	Phase relative to the clock, ns
datalink/LED	[16, 40]
DATAOUT0	[12, 33]
DATAOUT1	[12, 33]
TOKENOUT0	[14.5, 39]
TOKENOUT1	[14.5, 39]

An example histogram is given in Figure 4.

Input Signals Duty Cycles

The delay chips mentioned in the "Input Signals Phases" part have the additional ability to tune the delay for the negative signal edge. We use this feature to scan the duty cycles. In principle, all input signals duty cycles could be varied. At this time we only test the clocks.

The test system is capable of changing the duty cycle in the range of [0.35, 0.8]. We require that the corresponding test vector efficiency is 100% in the region [0.4,0.6] at 40 MHz.

The example histograms are not shown, since they are not interesting, having 100% efficiency in the range of the scan.

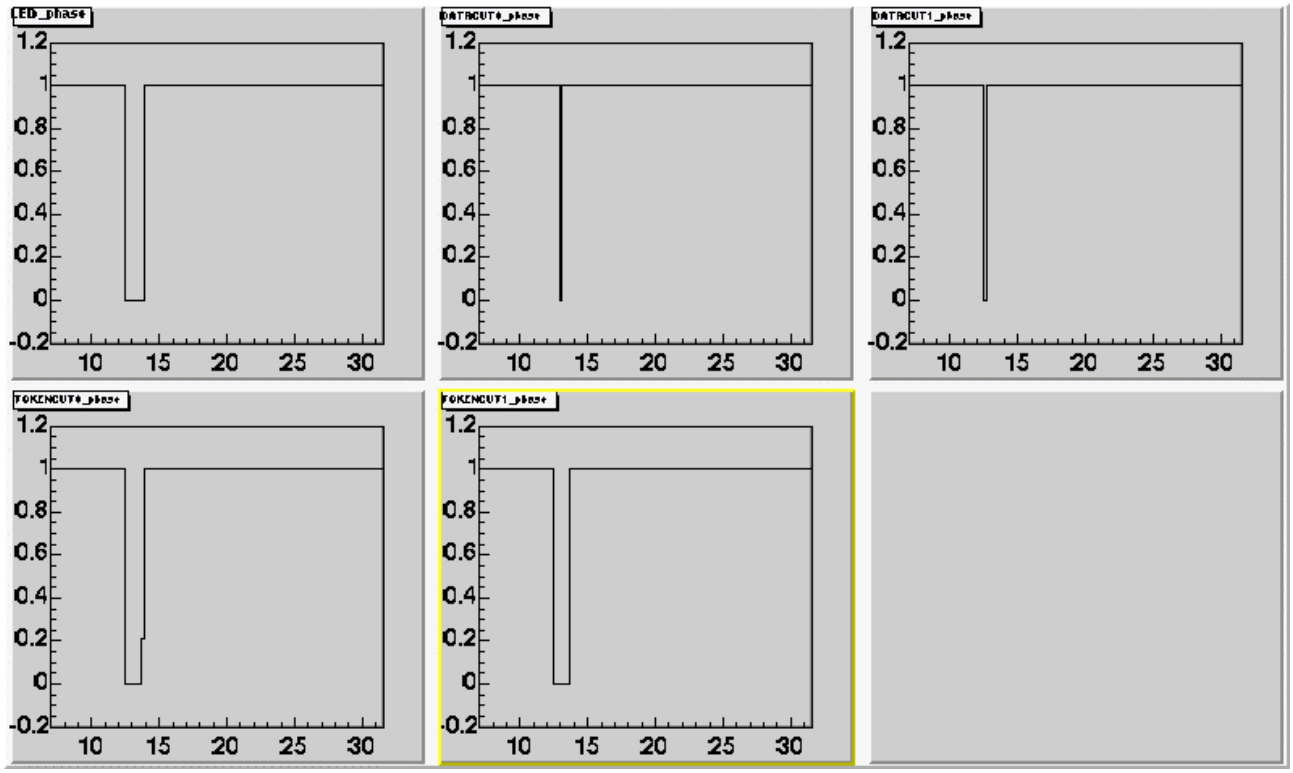


Figure 4 Output signal phases wrt clock. The histograms are the test vector efficiency as a function of the latching clock delay (in ns). The signal propagation time from the blue box to the probe card and back is not taken into account.

Output Signals Duty Cycles

This test has not been foreseen. Implementation would probably require a significant design change.

Conclusions and Status

We can test the signal levels and phases for input and output signals and duty cycles for the input signals. The input signal levels test has hardware limitations at low values of voltage swing. We cannot test the output signals duty cycles with the current scheme.

The "simple" diagnostic version of the software has been written (originally by Carlos). The process of integrating the tests in the main production framework is underway. The testing procedures imply simple offline analysis algorithms.