The testing time minimization estimates.

Vitaliy Fadeyev
September 10, 2001

The timing estimates were not available at the time of the testing time minimization discussion (phone meeting on August 31 ’01). The table below contains the actual numerics.

All the changes agreed-upon to be implemented during the "gray period" are shown. The latest (unofficial) software is used. The frequency step is 10 MHz, as during the preproduction screening.

The actions are:
(1) changing the number of triggers per analog point from 500 to 200,
(2) merging of the W4 test vector family,
(3) skipping the loop over Vdd range for frequency above 50 MHz (measurements are done at Vdd=3.7 V only),
(4) reducing number of TV passes from 100 to 10,
(5) addition of the "new" ABCD I/O signal tests.

Conditions	**Time per good chip, Min:Sec**	**Time per wafer, Hour:Min[1]**
Preproduction parameters	2:43	10:25
Preproduction parameters & (1)	2:19	8:54
Preproduction parameters & (1) & (2)	1:52	7:25
Preproduction parameters & (1) & (2) & (3)	1:22	5:15
Preproduction parameters & (1) & (2) & (3) & (4)	0:59	3:46
Preproduction parameters & (1) & (2) & (3) & (4) & (5)	1:08	4:21

[1] Assuming that there are 10% "DEAD" chips on a wafer