Preliminary Results of the I/O Tests Performance.

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The I/O signal tests are described in details elsewhere. The signal characteristics we test are summarized in Table 1.

Table 1 I/O signals tests and the extracted quantities.

Test Type	**Scanned Parameter**	**Extracted (Output) Quantity**
input phases	input signals delays	The value (and its error) of the extra time delay of the signal when the ABCD is having a signal latching problem.
output phases	output signal delays	The value (and its error) of the output signal time delay wrt the input clock.
input levels	swing of the input differential signals	Minimal value of the swing at which the test vector still works.
output levels	window comparators thresholds	The signal swing.
clocks duty cycles	duty cycles of the clocks supplied to the ABCD	The Minimal and Maximal working values of the clock duty cycle.

For each type of test and each signal, a test vector stimulating the signal is run and the tester parameters affecting the signal (time delay, swing, window comparator level, duty cycle) is scanned. The test vector efficiency indicates the working conditions. We measure the working regions for the input signal parameters and the values of the output signal parameters for a given chip.

The results are based on a partial wafer scan done at SCIPP probe station.
The tests results are only considered for chips which have 100% efficiency for all 10 test vectors at Vdd = 4.0V and F = 40 MHz (initial TV check).

The distribution of the input signals time delays causing latching problems in the chips (i.e. *non-working* regions central values) is shown in Figure 1.
The distribution of the output signals time delays wrt the input clocks is shown in Figure 2.
The distribution of the min. values of the input signal swings is not shown, since

all chips passing the initial TV check work at the minimal value the system can provide (65 mV).
The distribution of the output signals swings is shown in Figure 3.
The distribution of the clocks duty cycles min and max values is not shown, since all chips passing the initial TV check work in the full range the system can provide (from about 25% to about 75%).

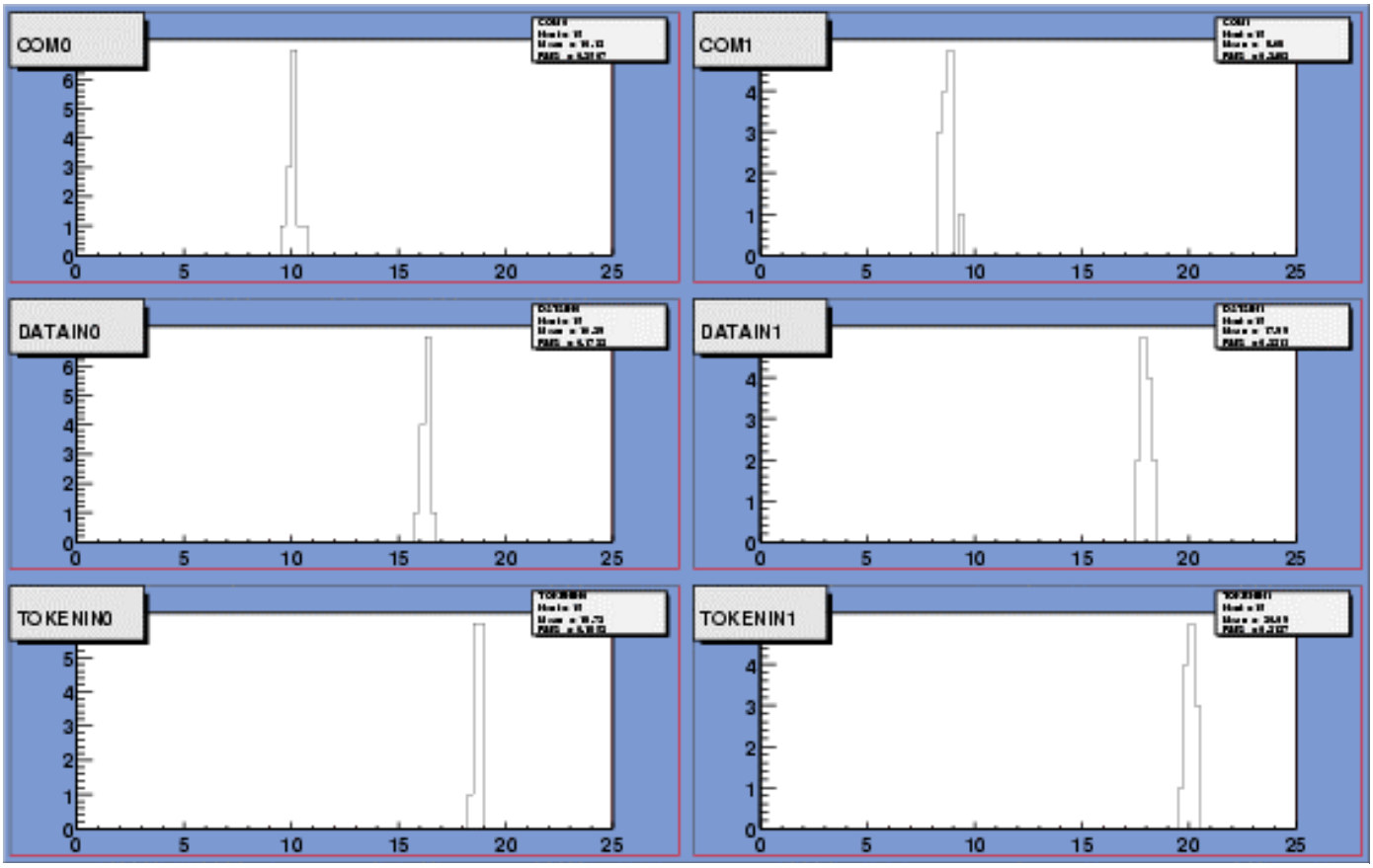

Figure 1 The distributions of the input signal delays causing the latching problems in the ABCD.

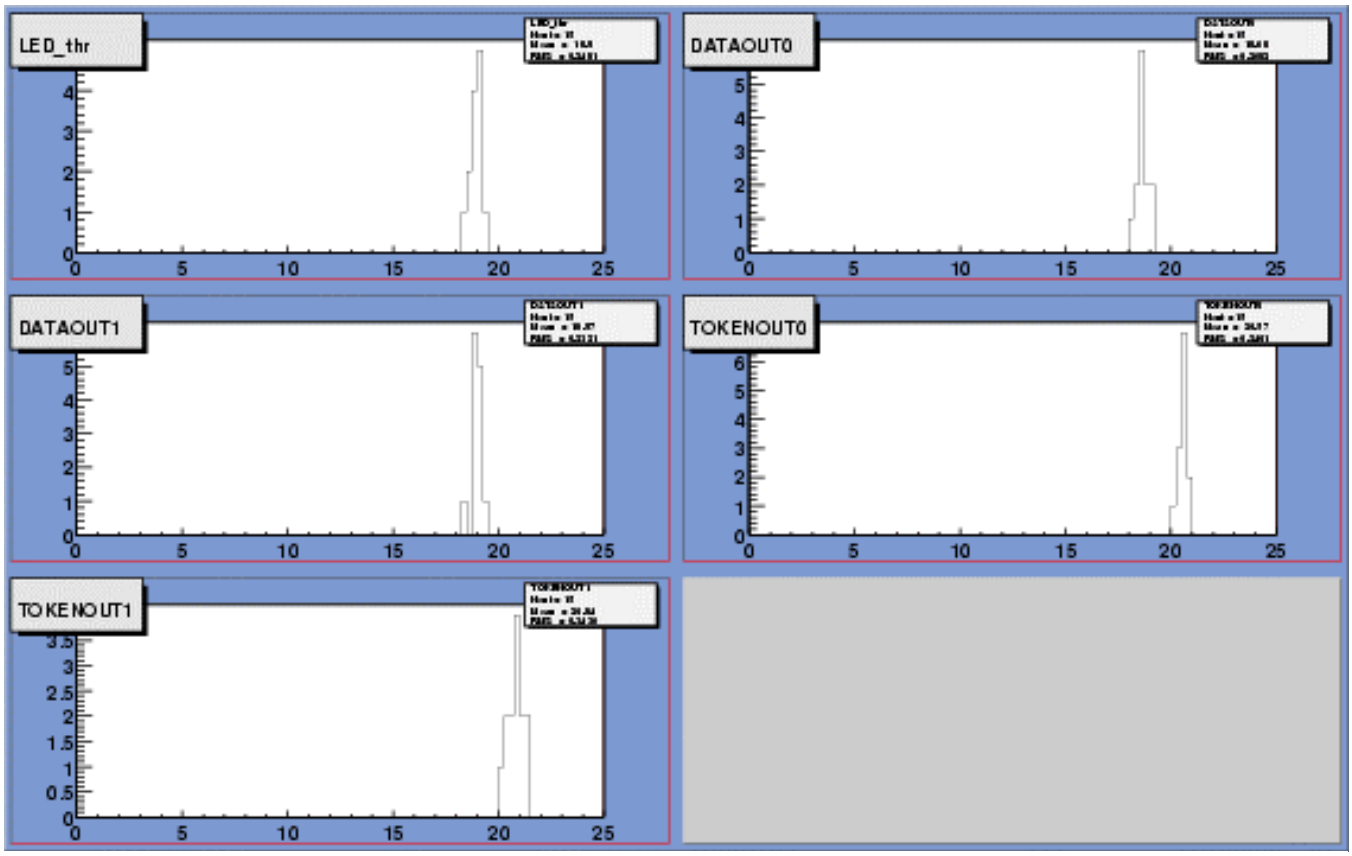

Figure 2 The ABCD output signals delays distribution wrt the rising edges of the input clocks, in ns.

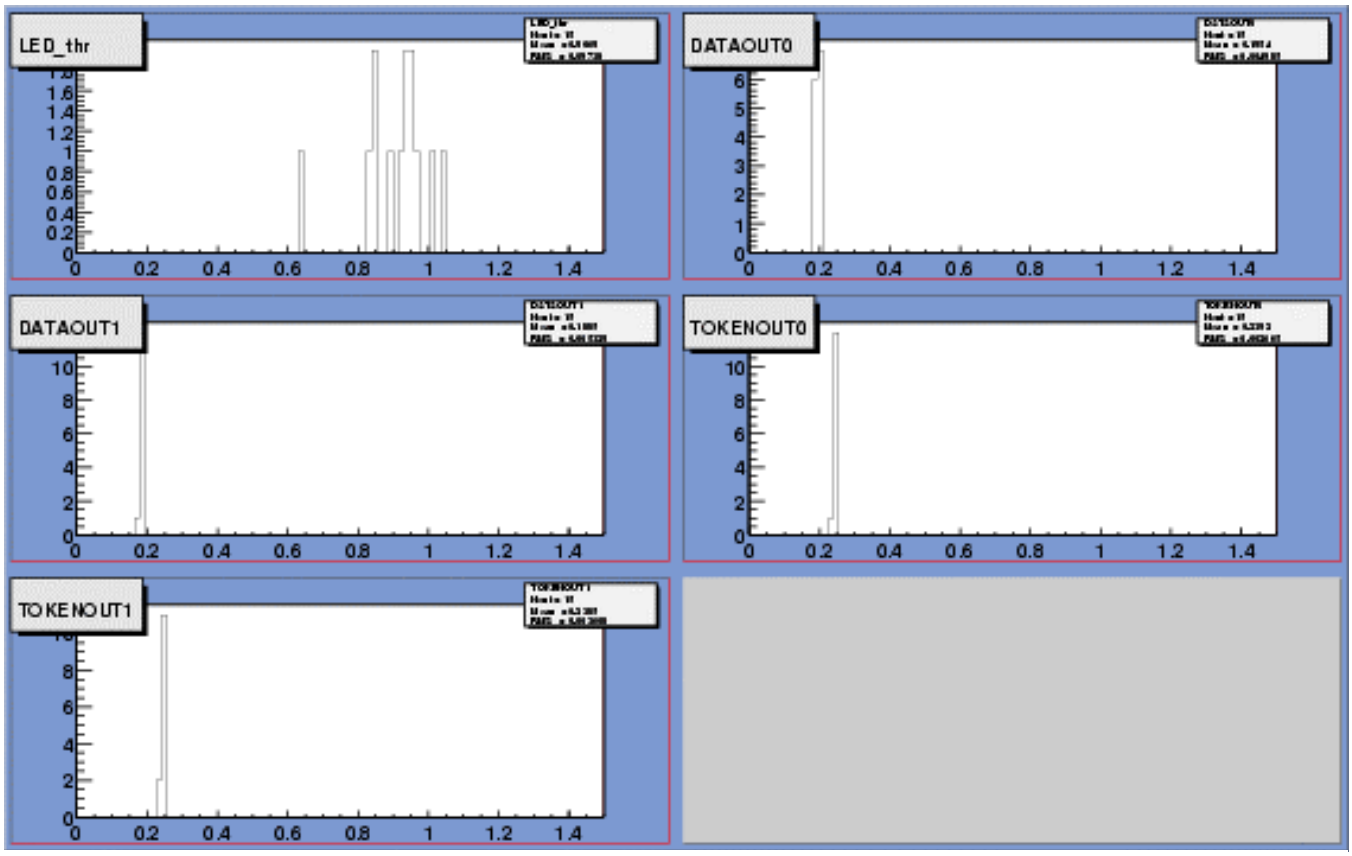

Figure 3 The distribution of the output signals swings, scaled by the factor of 3, in V.