# Proposed Procedure for Determining Optimal Calibration Strobe Delay

DRAFT 9/12/01

Max Wilder

The procedure for determining calibration strobe delay has not been standardized. CERN and SCIPP are using different procedures. I do not know what procedure RAL uses.
Since analog test results depend critically on the choice of strobe delay, we need a standard procedure to insure accuracy and reproducibility of results. The procedure should be mechanical if possible, and fast.

Threshold scans are currently performed using one strobe delay for all input charge values, and all thresholds. The delay should be chosen to give maximum efficiencies in the region of the 50% point where accuracy is critical, and good efficiencies at low thresholds. At high thresholds the efficiency is not critical since there is no data to speak of . "Efficiency" is defined here as the number of hits that are read out of the pipeline vs. the number of hits seen by the preamp/comparator circuit. In contrast, "occupancy" is the number of hits read out of the pipeline vs. the number of calibration strobes at a given input charge and threshold.

High efficiency occurs when the comparator output pulse has reached a plateau before being latched. This does not occur at a fixed time under all conditions. The timing and width of the comparator output pulse depends on the input charge and the threshold setting. For a fixed input charge, the output pulse will be delayed and narrow as the threshold is increased. For a fixed threshold, the output pulse will occur sooner, and widen as the input charge increases. These timing shifts will cause shifts in readout efficiency during a threshold scan.

Low efficiencies occur when the output pulse rising or falling edge is latched. In this case, noise can cause the edge to be larger or smaller than the latch threshold voltage. Efficiencies are also low if the timing is so far off that the pulse is not latched in the right timeslice.

Efficiency is also effected by the edge sensing option, data compression algorithm, and the VME board data acquisition program. In normal threshold scans, edge sensing is enabled, but hits are recognized in any of three timeslices by readout electronics, which mitigates timing issues. If data is missed in the middle timeslice, it may appear in the first or third.

The utility programs "Scan" and "HybScan" enable measurement of occupancy as a function of input charge, comparator threshold, and strobe delay. "Scan" takes the data, "HybScan" produces a root file. Together they provide enough information to select a suitable value for the strobe delay.

Strobe delay scans use a fixed input charge and threshold, and measure occupancy vs. the strobe delay. The Scan program also loops over threshold, producing one histogram per threshold value. It produces histograms for each channel, and also a composite histogram of all channels (called "AllChan" in the root file). We rely entirely on the AllChan histogram. For a full picture of the various timing shifts, it is useful to run strobe delay scans for each of the input charges used in threshold scans (2,5, 3, 3.5, 4.0 fC), using the full range of threshold values. In practice, only one scan is needed, the 4 fC scan, as will be explained below.

It is helpful to understand how the delay scan histogram corresponds to the comparator signal.

The delay scan starts at zero delay and increases to a maximum of 50 ns. Typically, at zero delay the data is not latched into the timeslice being read out. As the delay is increased, the falling edge of the pulse overlaps with the rising clock edge and data is latched. The efficiency rises as the falling edge and plateau sweep through the clock edge, and falls as the pulse rising edge passes the clock edge. In the strobe delay histograms, the left-hand side (rising edge) corresponds to the falling edge of the comparator pulse. The right hand side (falling edge) corresponds to the rising edge of the pulse.

The most critical area of the threshold scan is near the 50% point, and here we should insist on good efficiency. For a fixed input charge, with the threshold set near the 50% point, the delay scan histogram will show two or more peaks and troughs with 20=30% peak to trough variations in occupancy. The position of these peaks does not change much as input charge and threshold voltages vary, and therefore make useful timing marks.

An examination of a full set delay scans shows that the delay value at the rightmost peak of the 4 fC scan gives high occupancies at all input charges and thresholds. I propose to use this delay value for threshold scans. This peak corresponds to the comparator plateau just after the rising edge. The timing of this part of the signal is mainly a function of the RC-CR shaping time and should not be too dependent on time over threshold. A large input charge will take longer to peak than a small charge. It is advantageous to use the large signal peaking time because at that time smaller signals will have peaked and still be near maximum values. If the peaking time of a small signal is chosen, it may come on the rising edge of large signals, causing loss of efficiency.

The procedure employed at SCIPP is as follows:

1) Test 9 chips distributed about the wafer with digital tests to find at least 4 digitally perfect chips (at 40 and 50 MHz). If four are not found, test additional chips. We test more than one chip in case the optimal delay is not constant over the wafer. If data shows that the distribution is always tight then we will test fewer chips.
2) Run delay scans on each of the digital perfect chips using Scan. Input Charge is 4.0 fC, threshold range is set to bracket the likely 50% point. We don't have to get exactly 50% efficiencies because the peak positions are not much effected by threshold values.
3) Create root file with HybScan, open root, read in root file, and examine AllChan histogram directory. (this is a composite of all 128 channels. Histograms for each channel are also available.) There is one histogram for each threshold voltage. Choose the threshold value with efficiencies nearest 50% and record the delay value of the rightmost peak. Repeat for each of the chips tested.
4) Average peak values for all tested chips. Use average value for threshold scans.

This procedure takes about 45 minutes. For now we are testing every wafer once. If data shows that wafers within a lot have reasonably constant optimal delay, then we could test one wafer per lot.

I will circulate delay scan histograms and data over the next day or two. Any comments or criticisms will be gratefully accepted.