The "Fast Pipeline" Tests Description.

Version 1
Vitaliy Fadeyev
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The purpose of the Fast Pipeline tests is similar to the corresponding Test Vectors. Unlike the Digital Tests, the user receives more detailed information about the state of pipeline for all 128 channels.

The "Dynamic Pipeline test" is similar to W4TEST (aka "input register test"). For this test, the ABCD chip is initiated with the following configuration:
EDGE_DETECT | COMPRESS_LEVEL | MASK_DISABLE
The threshold voltage is maxed out.

The "Static Pipeline test" is similar to W6TEST (aka "input lines test"). For this test, the ABCD chips is initiated with the following configuration:
LEVEL | MASK_ENABLE
The threshold voltage is nominal.

The bulk of the tests is done in the same way as the analog tests. The calibration pulse command ("pulse input register" command in the case of the "Dynamic Pipeline test") is sent to the chip followed by a trigger command 144 times. The chip data are interpreted by the analog data decoding algorithm, the number of hits for each channel is stored in the VME board memories and then read out.

The trigger-to-trigger space is 1 clock cycle modulo 12, to test all pipeline rows.

Each of the tests is done 4 times, with different mask patterns:
"0000...",
"0101...",
"1010...",
"1111...".

The number of channels not confirming to the patterns expected is reported in the lower message field of the WfScan window.

At the analysis stage the data for each channel are classified in the following way:
-- "stuck low" (data are all zeros for all masks),
-- "stuck high" (the channel has hits for all masks),
-- "funny" (not stuck low, not stuck high and not confirming to the expectations),
-- "too efficient" (efficiency >100%, this category (included in the previous one) is made to trace a special rare case when chip has a problem with address encoding).

The number of channels falling into each category is stored in the Chip class. For a good chip they all should be zeros.

Summary:

-- the tests provide detailed information about the pipeline state for each channel,
-- the tests are fast, with sub-second execution time,
-- these tests run at 40 MHz only,
-- there is a possibility of the online selection (rejection of the bad chips).