Running TESTVECTORS

For testing the digital back-end of the ABCD chips, the functionality of running testvectors has been added.

This works as follows:

1) you store the testvector in the TV memory using the corresponding VME command.
2) The end of a testvector is marked by bit 17 being a 1, all other lines must have bit 17 set to 0.
3) To see which bit of the testvector corresponds to which signal, compare the pinout of the VME board with the schematic of the pin driver boards.
4) Write your simulation vector to the simulation vector memory.
5) Set frequency as described in the module part
6) Issue start signal
7) Then the TV is transferred at 40 MHz to the output fifo, then sent to the chip at the programmed frequency.
8) The chip response is read back into the resync fifo at the same time. The write clock for the resync fifo is the clock fed back from the pin driver board.
9) When the output fifo is empty, the content of the resync fifo is read by the fpga and compared with the content of the sim memory.
10) The comparison starts at the sequence (011101), which represents the header of a valid readout.
11) The result of the comparison is one bit of the fpga status register
12) You can read back the readout from the resync fifo by sending a “retransmit” command and do consecutive reads from the fifo.