How to program a Scan

Important: Before you issue any command, check with the "read status register" command (x00) that the busy flag is not set (bit 16)!

1) Initialize Module

- Set Frequency to 40 MHz (x0F)
- Set VCC and VDD DAC's (x0A)
- Load Configuration Register of all chips
- Load Mask Registers of all chips: For each chip, do the following
  - Reset Mask Register Pointer (x15)
  - Write 4 times to FPGA Mask Register (x16)
  - Load FPGA Mask Register to Chip (x17). It's here where you specify the chip address.
- Load Trim DAC's of all channels of all chips (x1E). That's 12x128 commands.
- Load Strobe Delay Register of all chips(x18)
- Load Bias DAC's of all chips(x1D)

2) Initialize Scan Parameters

- Clear Histogram Memory (x03)
- Set Number of Triggers per scan step ("burst") (x11) (observe the 1!)
- Set Trigger to Trigger delay (x10). This is the number of clock cycles between 2 consecutive L1 Trigger commands. Make sure you allow enough readout time.
- Set Strobe to Trigger delay (x1F). This should be around 129.

3) Do the Scan

Loop over the following 5 commands (i = [0..number of scan points-1])
- Load Configuration Register of all chips
- Enable Data Taking
- Set the scan parameter (eg. threshold) to the i-th scan point (eg. x19)
- Set base address to the actual step number i (x05)
- Send burst of triggers (x0E)

4) Read Histogram Memory

- Set base address to 0 (x05)
- Read from Histogram Memory (x04) for 512k times (or less if you have less chips).