Test System for ABCD3T Wafer Screening

1. Introduction.

An ASIC wafer test system has been developed to provide comprehensive production screening of the ATLAS Semiconductor Tracker front-end chip (ABCD3T). The ABCD3T features a 128-channel analog front-end, a digital pipeline, and communication circuitry, clocked at 40 MHz, which is the bunch crossing frequency at the LHC. The tester measures values and tolerance ranges of all critical IC parameters, including DC parameters, electronic noise, time resolution, clock levels and clock timing. The tester is controlled by an FPGA (ORCA3T) programmed to issue the input commands to the IC and to interpret the output data. This allows the high-speed wafer-level IC testing necessary to meet the production schedule. To characterize signal amplitudes and phase margins, the tester utilizes pin-driver, delay, and DAC chips, which control the amplitudes and delays of signals sent to the IC. Output signals from the IC go through window comparator chips to measure their levels. A probe card has been designed specifically to reduce pick-up noise that can affect the measurements. The system can operate at frequencies up to 100 MHz to study the speed limits of the digital circuitry before and after radiation damage.

2. System Description.

2.1. Testing Requirements.

The ABCD3T[1], which operates at 40 MHz, features a 128-channel analog front-end consisting of amplifiers and comparators, and a digital pipeline and communication circuitry. To reduce power consumption and cost, the IC utilizes a binary readout scheme where the signals from the silicon detector are amplified and then compared to a threshold. Only the result of this comparison based on a hit or no-hit logic is stored in the digital pipeline. Internal 3-bit DACs to trim the threshold are part of each readout channel to correct for the gain and threshold variations both before and after radiation damage. The analog circuitry of the chip is calibrated via a charge injection method.

The basic method for the characterization of the analog circuitry of the ABCD3T consists of an efficiency scan for different threshold values with a fixed calibration charge. A typical “S-curve” from this measurement is shown in Fig. 1. The 50% point indicates the threshold value and the width characterizes the noise. To extract the gain and offsets, the scan is done at different calibration input charges. To characterize the trim DACs, the scan must be done for all the different DAC values. All of these procedures can be performed automatically for each of the 128 channels (Figures 2,3) on every IC on the wafer. To avoid long testing times, the histograms of the data from the chip are calculated in hardware.

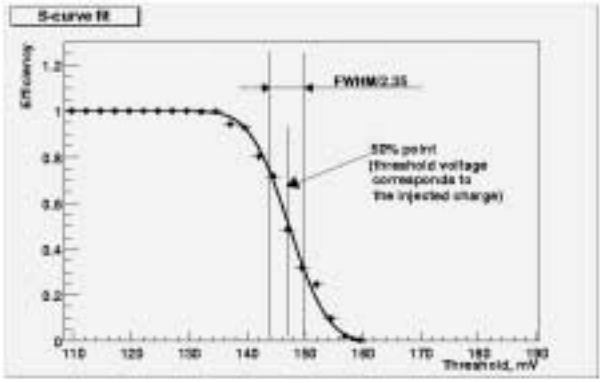

Figure 1. *S-curve for a single channel.*

The digital part of the chip includes redundancy and data bypassing circuitry, to mitigate the effect of circuit failure in the high radiation environment of the LHC. The functions of the digital circuitry of the IC are verified using test vectors, which define the sequence of the IC’s control line values for consecutive clock cycles. The IC’s output signals are received by the FPGA and compared with the expected data corresponding to that particular test vector. Only the result of the comparison is read out. It has been shown that the radiation damage slows some digital circuits. Thus the ABCD3T should operate at frequency well above 40 MHz before irradiation. To evaluate ABCD3T performance after irradiation, the test vectors are run at frequencies higher than the nominal 40 MHz.

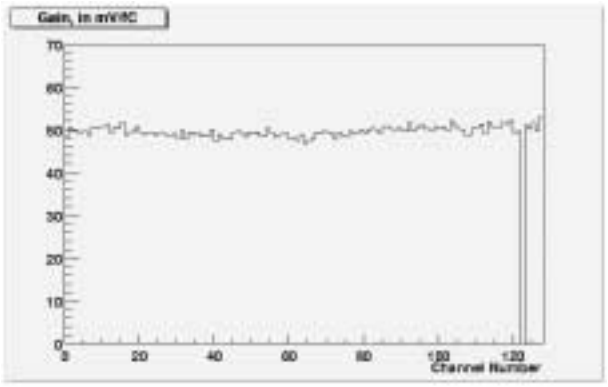

Figure 2. *Gain in mV/fC for 128 channels*

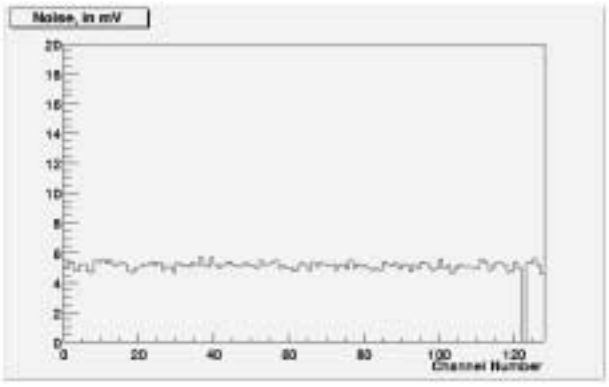

Figure 3. *Noise in mV of 128 channels of one ABCD3T*

To satisfy the schedule for the construction of the ATLAS SCT, the required wafer screening production rate exceeds two wafers per day per testing site (65536 channels). Therefore a very fast system is required.

2.2 Layout of the Test System.

The ASIC wafer test system[2], which consists of several custom designed PC boards and control software, has been conceived and built to meet all of the ABCD3T testing requirements (Fig. 4).

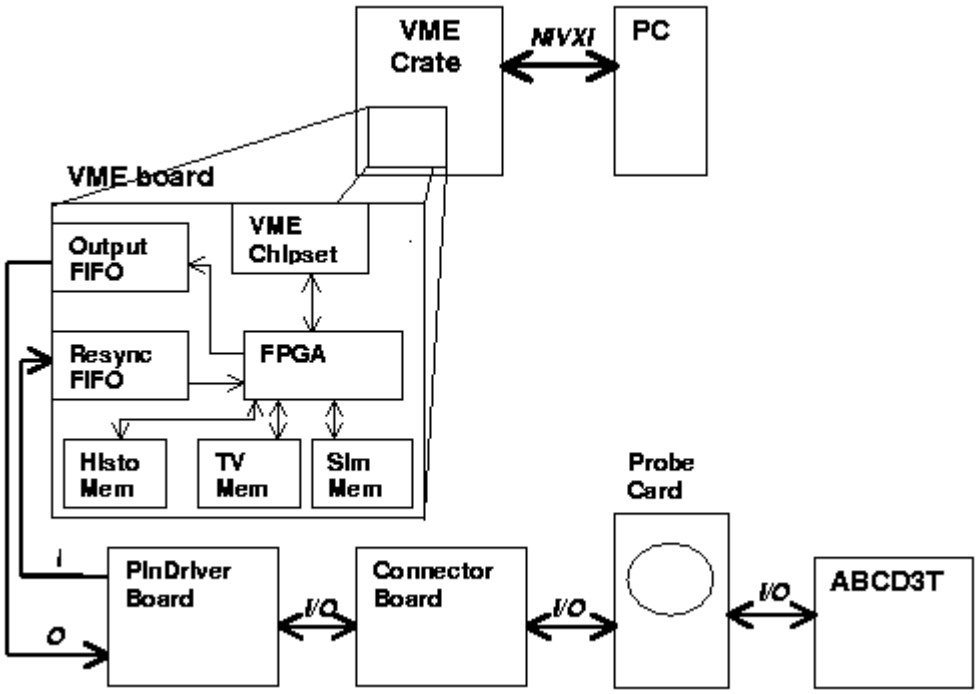

Figure 4. *Architecture of the ASIC test system*

A custom-designed VME board is equipped with an ORCA3T FPGA of 186000 gates, operating at 40 MHz and programmed in VHDL[3].
The main FPGA functions are:

1) To interpret VME commands and generate the bit-streams to be sent to the ABCD3T
2) To interpret the bitstream produced by the ABCD3T during the analog calibration procedure and store the histogram of hits in a dedicated memory chip on the board
3) To store a test vector and the simulated response (simulation vector) of the chip in a memory on the board, to send the test vector to the chip, compare the chip response with the simulation vector and provide the result of the comparison. This procedure is used for digital testing of the ABCD3T.

The test vectors can be run at higher frequencies than the nominal 40 MHz (up to 100 MHz).
This capability is achieved by buffering the signals in FIFOs, which allow for different frequencies of read/write operations. The higher frequency is obtained using a phase lock loop circuit on the VME board. The frequency is set by the FPGA.
Additional details of the functionality of the VME board can be found in Appendix A.
The data between the VME board and the probe card are transmitted as differential signals. Two intermediate boards[4] have been designed and built to provide:

1) High current pin drivers for inputs with variable signal level
2) Signal delays
3) Window comparators discriminating on the upper and lower output signal levels
4) Dedicated ADCs to probe the internal ABCD3T parameters; power consumption and feedback control of voltages supplied to the chip and ambient temperature of the pin driver board.

For all signals, the pin-driver and window comparator levels and delays are controlled by the FPGA via dedicated DACs.
A probe card[5] has been designed specifically to reduce the pick-up noise that can affect the analog measurements. Digital and analog signals are separated on different planes. An analog ground layer as well as a split digital/analog ground layer are used and low frequency filters are applied to the differential lines that control the analog part of the chip. All the decoupling capacitors are located as close as possible to the probe pins.

2.3. Implementation

The system is run on a PC under Microsoft Windows (W95/NT/2000). The PC communicates with the VME crate using the NI-VXI interface from National Instruments. The system is controlled by a Windows GUI written in Visual C++. The program is interfaced to ROOT[6], which does the curve fitting and data analysis. The information is stored in data files and processed to determine the yield.
The time needed to test one wafer containing 256 ABCD3T chips is about 5 hours. A recent study on the optimization of the testing parameters, in particular for the analogue test, can be found in Appendix B.
The ASIC wafer test system will be used at the following three ATLAS Semiconductor Tracker institutions: Univ. of California at Santa Cruz, CERN and Rutherford Appleton Laboratory.

3. References.

[1] ABCD3T ASIC Specification, http://chipinfo.web.cern.ch/chipinfo/docs/abcd3t_spec_v1.2.pdf
[2] http://www-atlas.lbl.gov/strips/tester
[3] http://www-atlas.lbl.gov/strips/tester/VME
[4] http://www-atlas.lbl.gov/strips/tester/pin_driver
[5] http://www-atlas.lbl.gov/strips/tester/probe-card
[6] Root: An Object Oriented Data Analysis Framework, http://root.cern.ch/