Test System for ATLAS SCT IC's and Modules

What we need to do

- next half year (prototype testing)
- in production

Setups, Measurements

Functionality of test system

Ideas for a new chip & module test system

Limitations of present systems

Open questions/discussion

ABC/CAFE-P & ABCD Prototype Evaluation 1999

Wafer Level Chip Tests
- Design Verification
- Production Spread & Yield

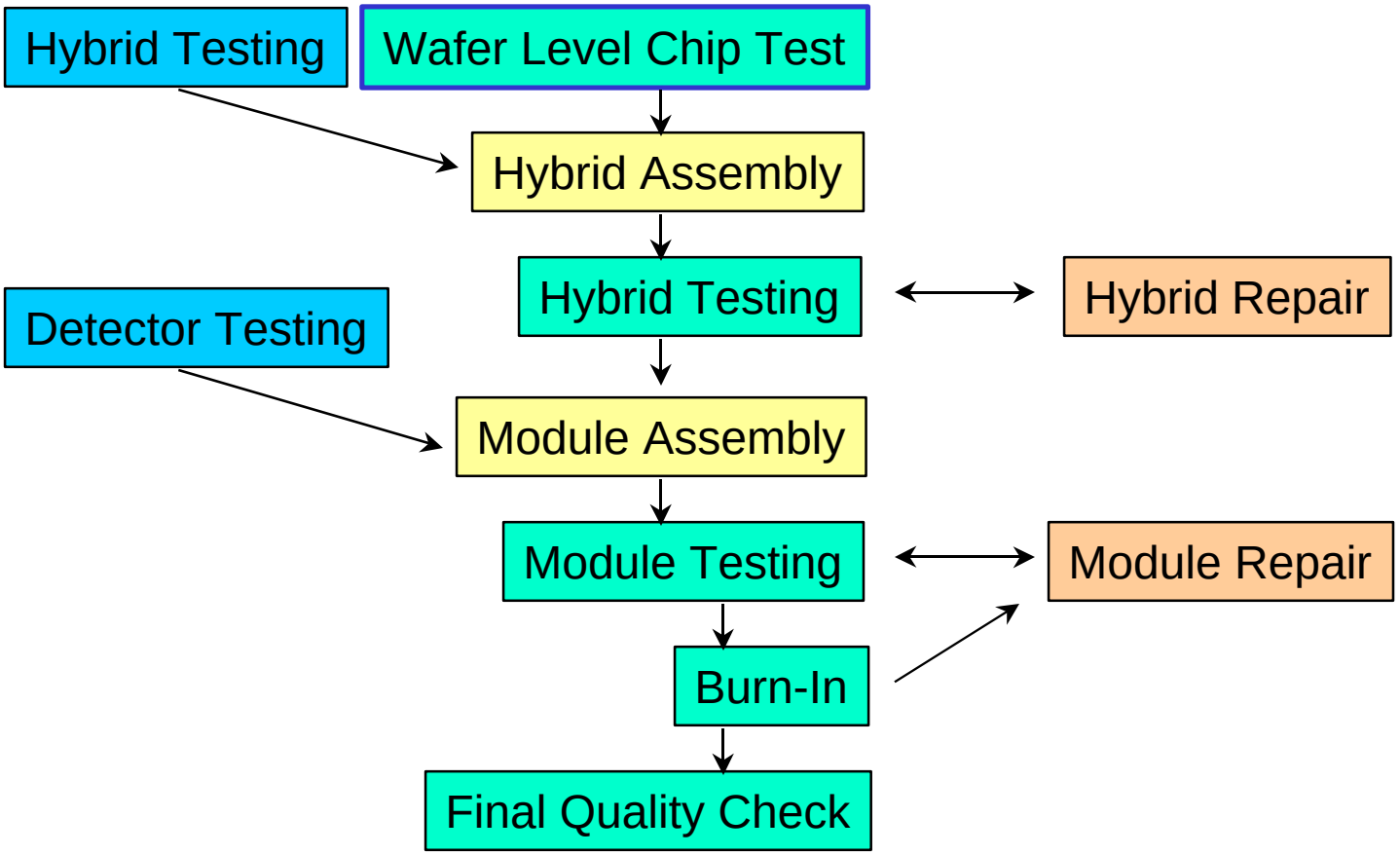
Assembled Hybrids
- Functionality & Performance

Irradiation Tests
- Single ABCD or ABC/CAFE-pairs
- Performance Analog & Digital
- Spread in Radiation Damage

Modules: Complete Characterization
- Threshold Scans..
- Laser, Source
- Testbeam (non-irrad. & irrad. modules)

Goals
- Choice of readout chips
- Final specifications for pre-rad wafer level chip tests
- hybrid technology choice or final justification of it
- Readiness for building small number of identical modules for PRR

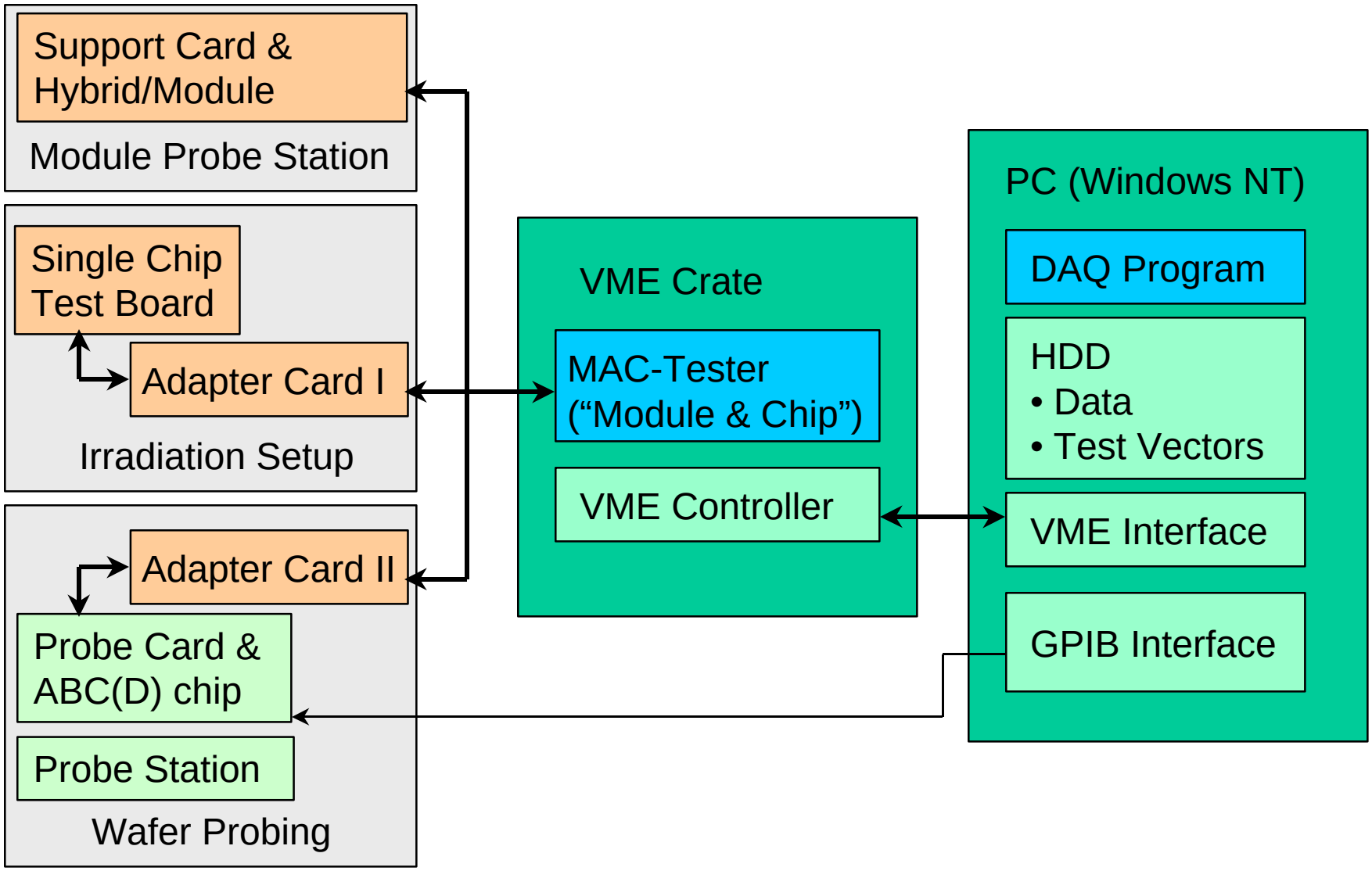
Production Testing



Test Setup's

Setup	Used For
Automatic Wafer Probe Station	Chip Testing
Portable Test System for Chip Irradiations	Testing of single chips (like wafer tests): Ana. & Dig. Performance during irrad.
Module Probe Station	Hybrid Testing Module Testing and Diagnosis
Test Beam	Simultaneous Readout of several Mod.
Active Burn-In Tester	Simultaneous Test of Reliability of many Modules

Test Systems Overview



Chip on Wafer Testing: ABC I/O Signals

8 LVDS input signals (programmable offset and amplitude)
(tokenIn0, tokenIn1, dataIn0, dataIn1, com0, com1, clk0, clk1)
8 CMOS input signals (not critical to timing)
(clkselect, resetB, masterB, id<4:0>)
5 LVDS (current mode) output signals (discriminate 2 levels/measure levels)
(ledout, tokenOut0, tokenOut1, dataOut0, dataOut1)
2 CMOS output signals
(calmode<0:1>)
1 (small) differential voltage output signal (discriminate levels)
(CALSP/N)
3 DC current level inputs (freely programmable)
(idar, inrh, inrl)
2 DC current level outputs (measure)
(cali, ith)
2 additional CMOS input signals for test-multiplexer and 1 CMOS output (?)
1 additional DC level input (CA)
Supply Voltage (VDD) and GND (programmable)

Chip on Wafer Testing

- Verification of VERILOG Model
- Test of all functionalities (DAC's etc)
- Measure parameter space in which chips are functional

Need to create 8 bitstreams with
- programmable delay
- programmable amplitude/offset of the signal

Another 8 bitstreams with fixed output signal phase/amplitude/offset
Receive 8 bitstreams (programmable discriminators)
Source 4 programmable (small) currents
Measure 2 currents

Basic Mode: Send out bitstreams, read chip response, transfer to disk

On-board comparison of chip response to test vectors with VERILOG simulation

Large number of test vectors O(100'000) with length around 1k

Operating frequency 60 MHz, better more. Frequency programmable.

Chip on Wafer Testing: ABCD

Additional Requirements

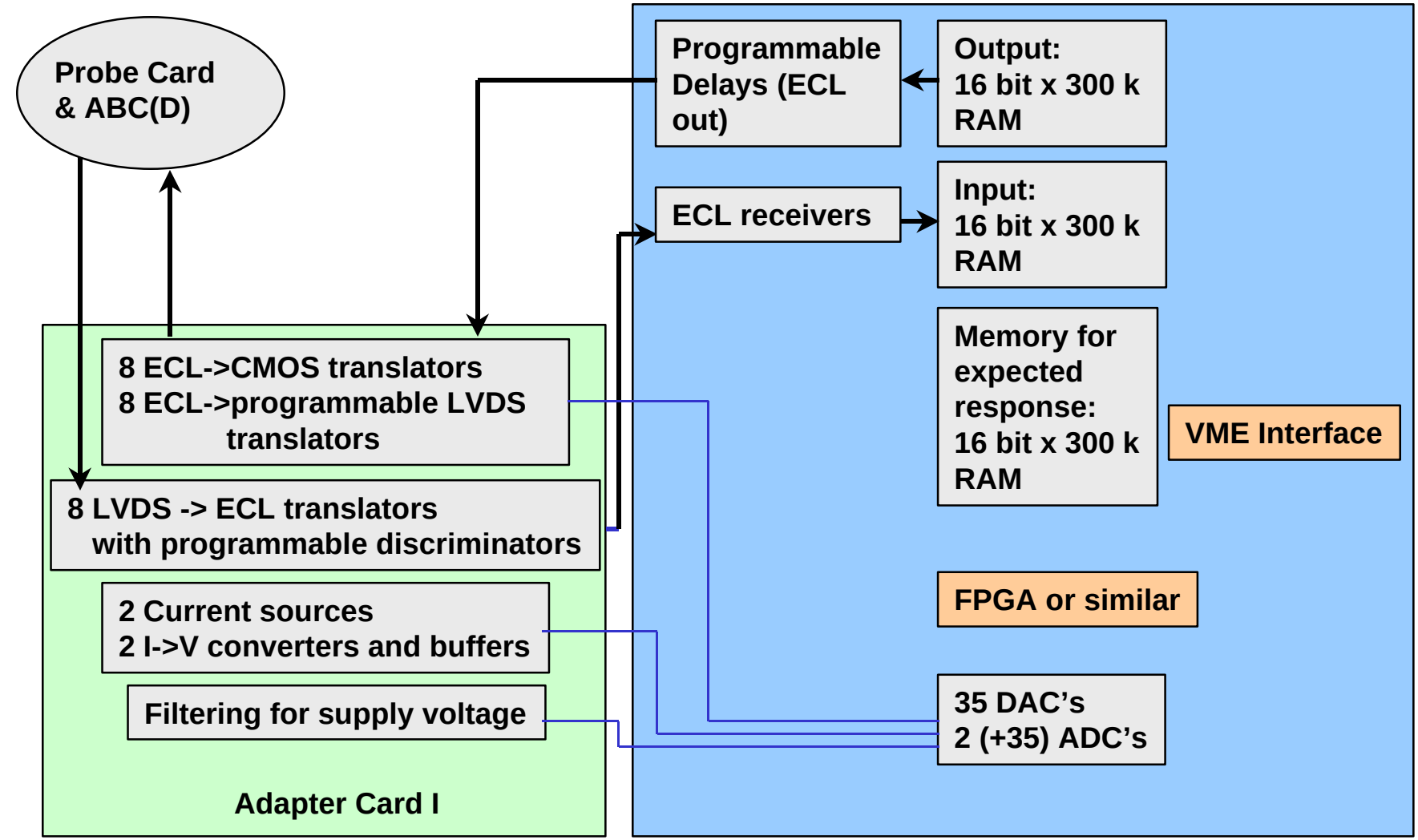
ABCD features:
3 DC voltage inputs
(VCC,Vt1,Vt2,)
2 DC voltage outputs
(Ipprobe, Isprobe)
4 analog signal inputs (calibration bus)

→ Need
- 3 programmable DC voltages
- measure 2 DC voltages
- generate 4 programmable pulses

ABCD has less analog I/O than ABC -> can be accounted for on adapter board
ONLY new feature is calibration bus -> needed also for hybrid/module test

A complete ABC test system contains all ingredients for an ABCD test system

Chip on Wafer Testing: Functional Block Diagram



Basic Modes of Operation

“AUTO-LOOP”: For debugging. Watch chip response on oscilloscope

•Test vector and it’s length written from PC to MAC tester.
• Set all DAC’s
• Send START signal from PC to tester
• Repeat sending test pattern to adapter card until signaled by PC to stop

“READ ONE VECTOR”: For debugging

•Test vector and it’s length written from PC to MAC tester.
• Set all DAC’s
• Send START signal from PC to tester
• Start sending test pattern to adapter card and reading data into fifo/memory
• Counter reaches length of test vector: Stop
• Read fifo/memory to PC

“RELIABILITY TEST MODE”

• Test vector and it’s length written from PC to MAC tester.
• Write “expected response” to memory
• Set all DAC’s
• Send START signal from PC to tester
• Start sending test pattern to adapter card and reading data into fifo/memory
• Compare with memory content during readout.
• If no error found in whole pattern, increment counter A, else counter B
• Stop if counter A or B reaches certain value or PC sends stop signal
• counters must be readable from PC during operation

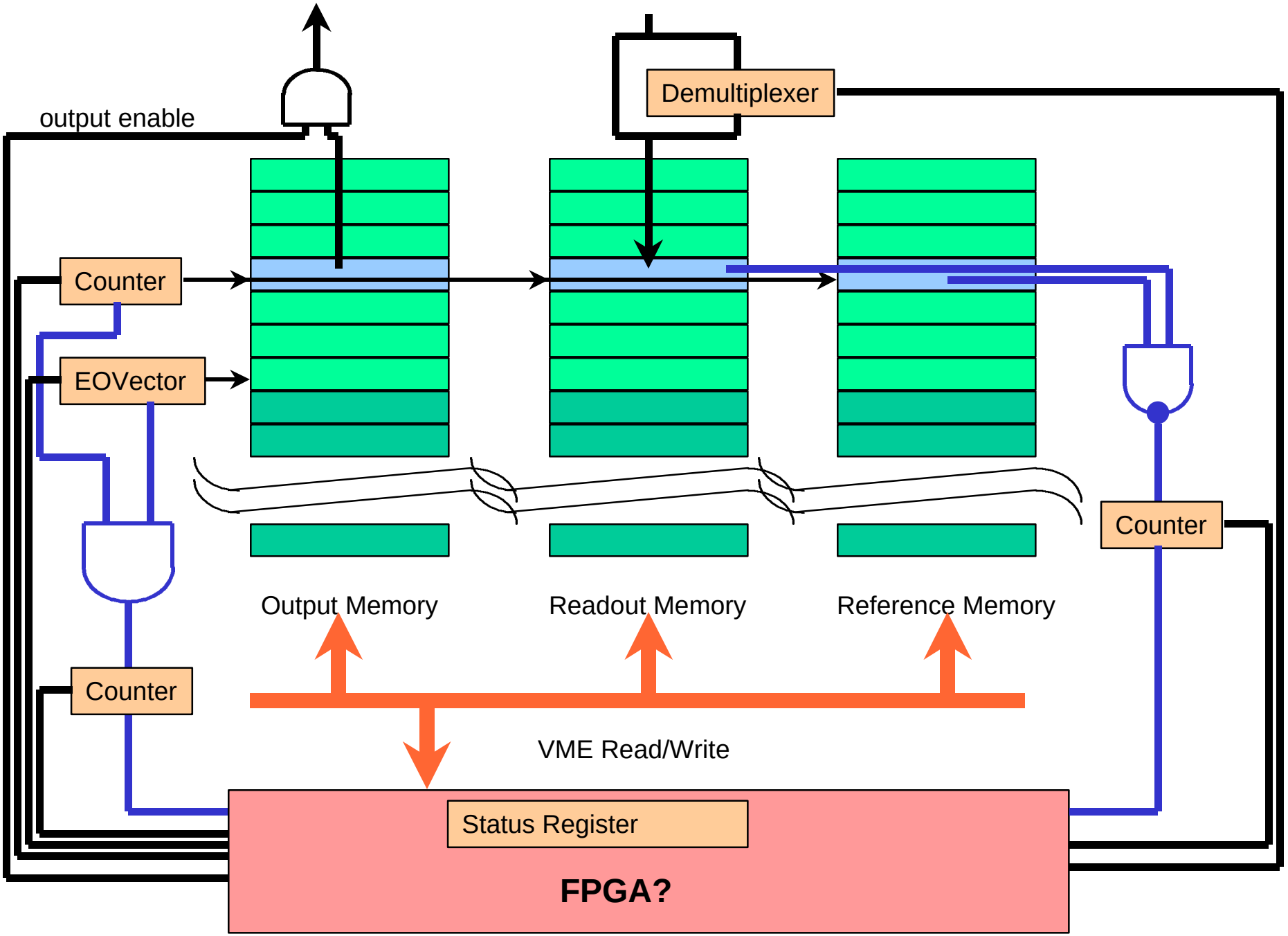
Basic Modes of Operation

“COMPARE AND STOP”

- Test vector and it’s length written from PC to MAC tester.
- Write “expected response” to memory
- Set all DAC’s
- Send START signal from PC to tester
- Start sending test pattern to adapter card and reading data into fifo/memory
- Compare with memory content during readout.
- Stop at end of test vector or repeat for a programmable number of times
- Set Flag if discrepancy found
- Possibility to Read out to PC

“THRESHOLD SCAN etc (ABCD)” == “READ ONE VECTOR”, except:

- Only 1 data stream needs to be read out and packed into memory


output enable
Demultiplexer
Counter
EOVector
Counter
Output Memory
Readout Memory
Reference Memory
Counter
VME Read/Write
Status Register
FPGA?

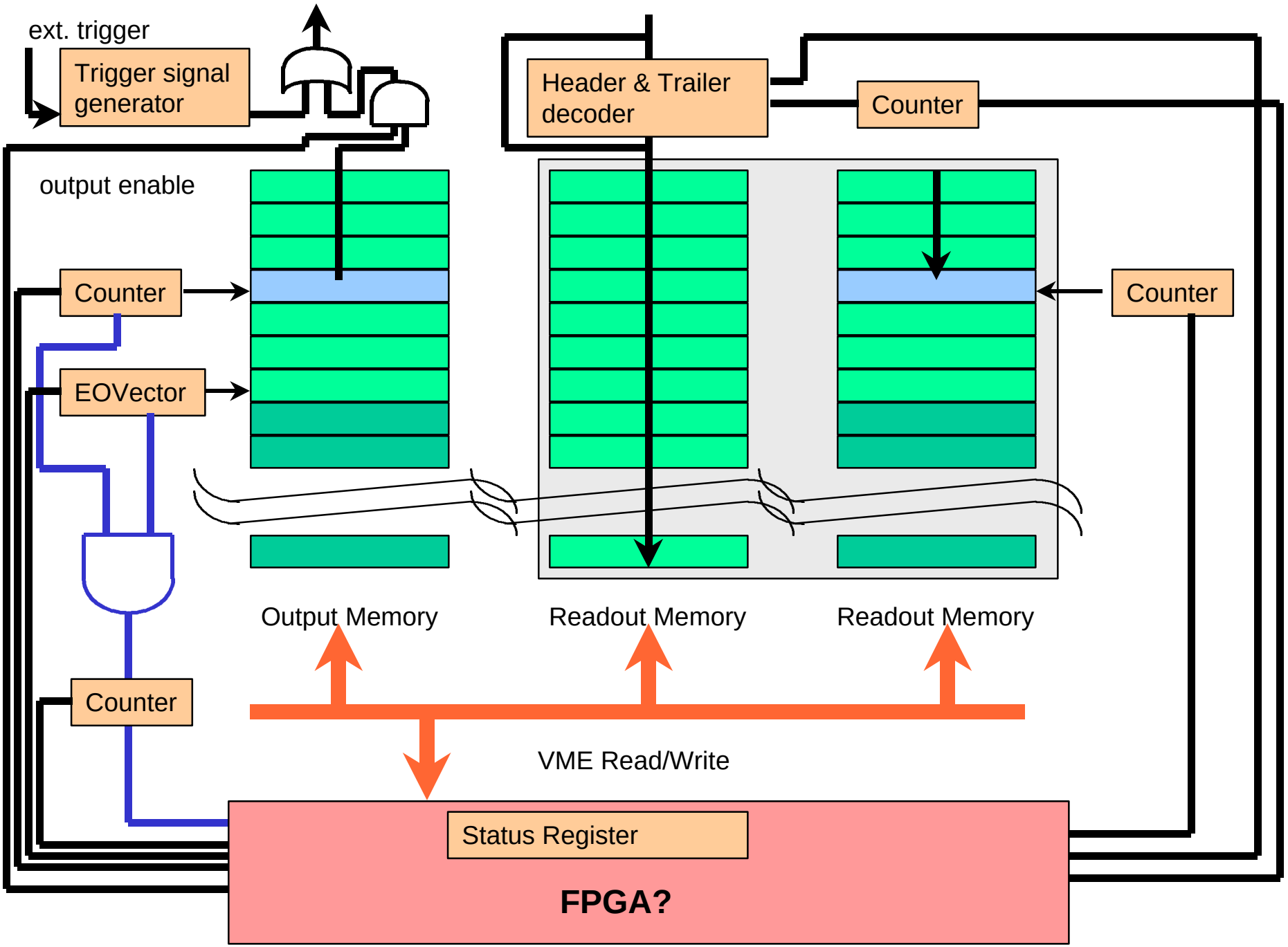
Hybrid and Module Testing

- Verification of VERILOG Model
- Test of all functionalities
- Measure parameter space in which hybrids/modules are functional
- Measure Analog Performance
- Portable System for testing during irradiation

- Same testmodes as for wafer testing
- Additional Requirements:
  - Create programmable voltages/currents for analog frontend
  - Create or pass HV for module(s)
  - External pulses (4 programmable pulses)
  - Create Trigger for Laser Pulser
  - Accept external trigger for measurements with radioactive source (fixed number of events/buffer overflow)

- Readout several Modules on external trigger
- Deadtime free at low trigger rate
- Allow to store 10’000 events for operation at highest trigger rate

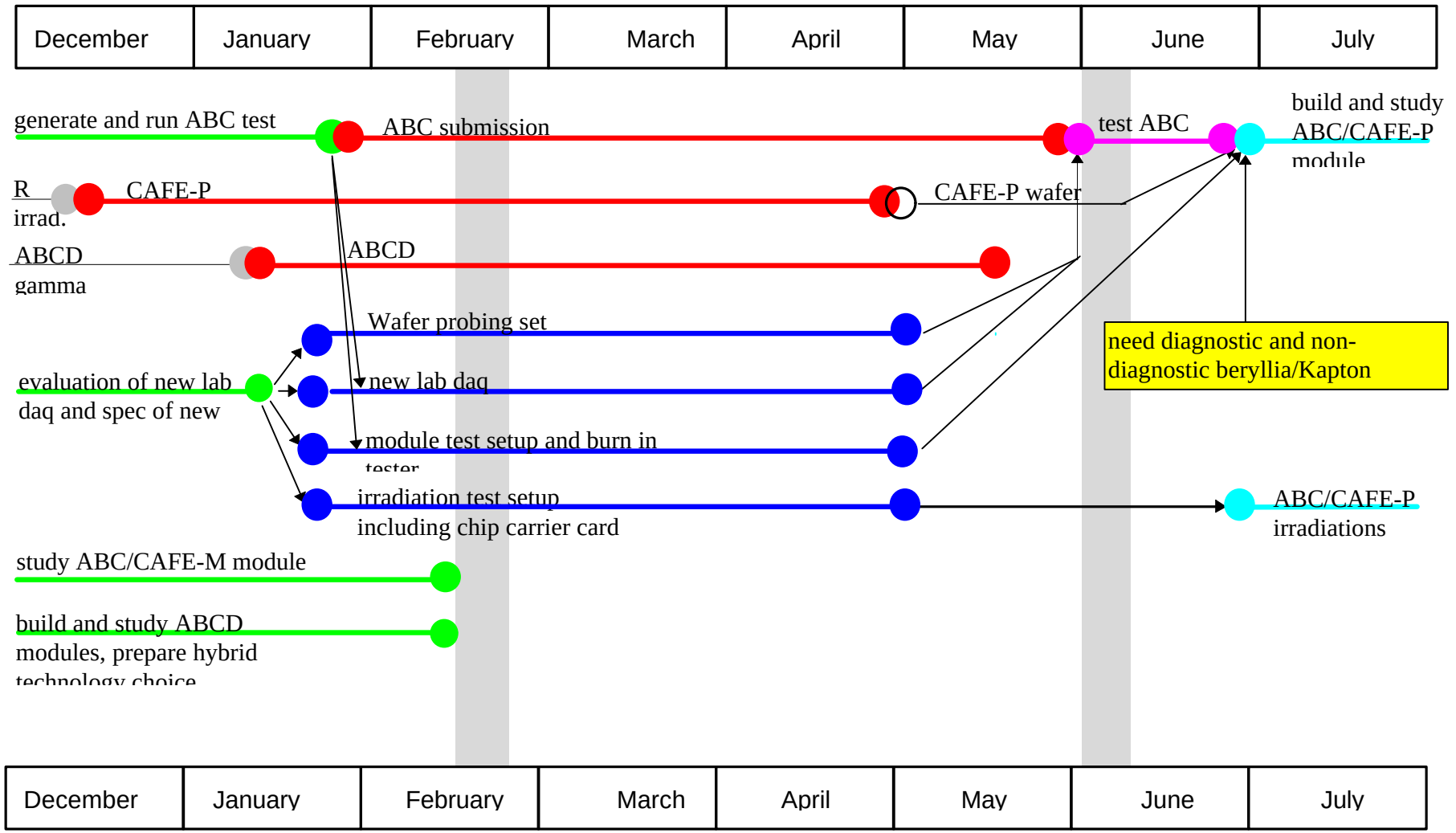
- All of the above
- Additional Requirements:
  - 8 Modules
  - Readout during data acquisition for low rate (deadtime free)
    -> swap between two memories (?)
  - Burst Mode for high trigger rates


ext. trigger
Trigger signal generator
Header & Trailer decoder
Counter
output enable
Counter
Counter
EOVector
Output Memory
Readout Memory
Readout Memory
Counter
VME Read/Write
Status Register
FPGA?

Test Beam and Burn-In Testing

With few additional features:

- Board can read out O(1500) events for 8 modules in burst mode (for 200kWords deep memory)
- Trigger frequency limitation in continuous readout mode is given by VME bus/disk access
- System can be used for burn-in testing of 8 modules


December
January
February
March
April
May
June
July
generate and run ABC test
ABC submission
test ABC
build and study ABC/CAFE-P module
R irrad.
CAFE-P
CAFE-P wafer
ABCD gamma
ABCD
Wafer probing set
need diagnostic and non-diagnostic beryllia/Kapton
evaluation of new lab daq and spec of new
new lab daq
module test setup and burn in tester
irradiation test setup including chip carrier card
ABC/CAFE-P irradiations
study ABC/CAFE-M module
build and study ABCD modules, prepare hybrid technology choice
December
January
February
March
April
May
June
July

Why new system?

Present systems (DSP, CDF PATT, RAL setup, CERN ASIC tester) have following major limitations

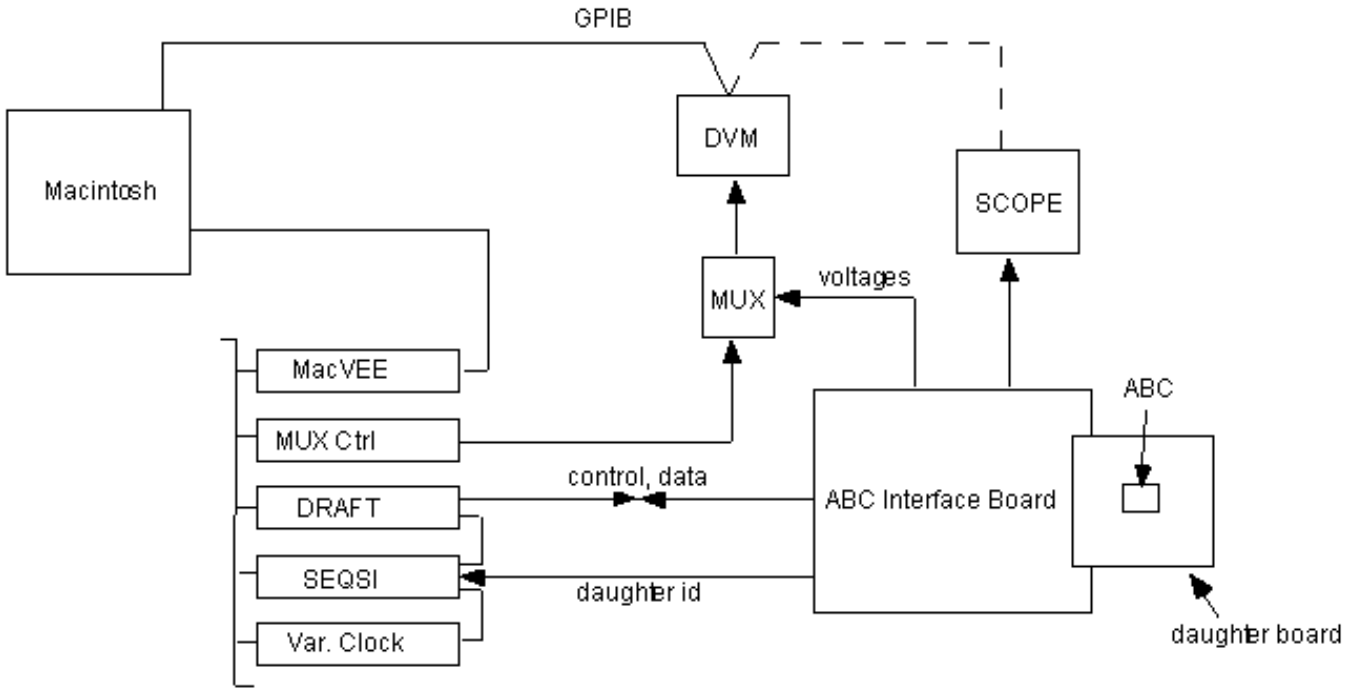
- max operating frequency too slow (all except ASIC tester)
- no data comparison on board (all except ASIC tester)

plus the following

- too specialized (ASIC tester, CDF PATT, RAL setup)
- memory too small and unflexible (all except DSP)
- not enough simultaneous I/O (DSP)
- CAMAC module (CDF PATT)
- none has enough DAC's
- more user friendly DAQ program needed

etc.

RAL ABC test setup



Open Questions

Feasible?

- Concept ok?
- Schedule?

Who has know how?

- “FPGA”, VME interface (hardware), analog part
- VME interface (software), DAQ program
- measurement requirements

Who is doing what?

Availability of Equipment?

- Probe station

New Equipment?

- Oscilloscope, power supplies, LabWindows(?), C++ compiler, GPIB interface