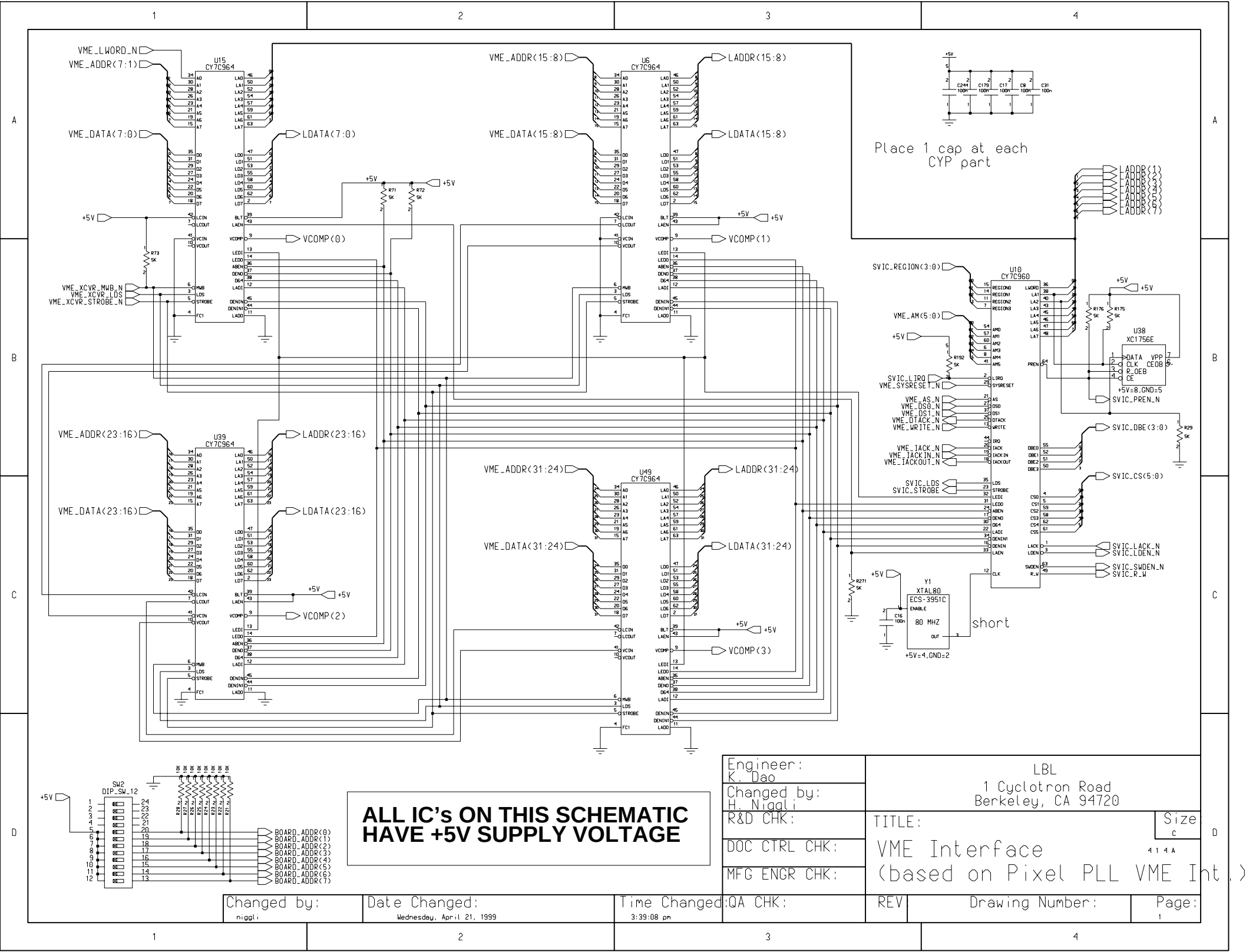
VME_LWORD_N
VME_ADDR(7:1)
U15
CY7C964
VME_DATA(7:0)
LDATA(7:0)
+5V
R71
5K
R72
5K
R73
5K
VCOMP(0)
VME_XCVR_MWB_N
VME_XCVR_LDS
VME_XCVR_STROBE_N
VME_ADDR(15:8)
U6
CY7C964
LADDR(15:8)
VME_DATA(15:8)
LDATA(15:8)
VCOMP(1)
VME_ADDR(23:16)
U39
CY7C964
LADDR(23:16)
VME_DATA(23:16)
LDATA(23:16)
VCOMP(2)
VME_ADDR(31:24)
U49
CY7C964
LADDR(31:24)
VME_DATA(31:24)
LDATA(31:24)
VCOMP(3)
Place 1 cap at each CYP part
C244 100n
C179 100n
C17 100n
C8 100n
C31 100n
LADDR(1)
LADDR(2)
LADDR(3)
LADDR(4)
LADDR(5)
LADDR(6)
LADDR(7)
SVIC_REGION(3:0)
U10
CY7C960
VME_AM(5:0)
R192
5K
SVIC_LIRQ
VME_SYSRESET_N
VME_AS_N
VME_DS0_N
VME_DS1_N
VME_DTACK_N
VME_WRITE_N
VME_IACK_N
VME_IACKIN_N
VME_IACKOUT_N
SVIC_LDS
SVIC_STROBE
R176
5K
R175
5K
U38
XC1756E
DATA
CLK
R_OEB
CE
VPP
CEOB
+5V=8,GND=5
SVIC_PREN_N
SVIC_DBE(3:0)
R29
5K
SVIC_CS(5:0)
SVIC_LACK_N
SVIC_LDEN_N
SVIC_SWDEN_N
SVIC_R_W
R271
5K
Y1
XTAL80
ECS-3951C
ENABLE
80 MHZ
OUT
C16
100n
short
+5V=4,GND=2
SW2
DIP_SW_12
10K
BOARD_ADDR(0)
BOARD_ADDR(1)
BOARD_ADDR(2)
BOARD_ADDR(3)
BOARD_ADDR(4)
BOARD_ADDR(5)
BOARD_ADDR(6)
BOARD_ADDR(7)
ALL IC's ON THIS SCHEMATIC HAVE +5V SUPPLY VOLTAGE
Engineer: K. Dao
Changed by: H. Niggli
R&D CHK:
DOC CTRL CHK:
MFG ENGR CHK:
LBL
1 Cyclotron Road
Berkeley, CA 94720
TITLE:
VME Interface
(based on Pixel PLL VME Int.)
Size
c
4144
Changed by: niggli
Date Changed: Wednesday, April 21, 1999
Time Changed: 3:39:08 pm
QA CHK:
REV
Drawing Number:
Page: 1