

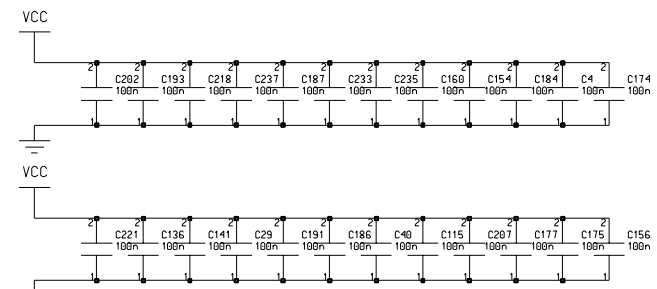
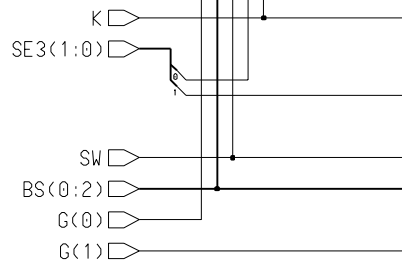
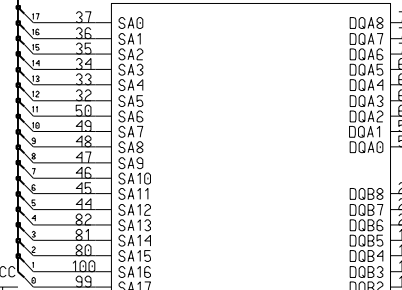
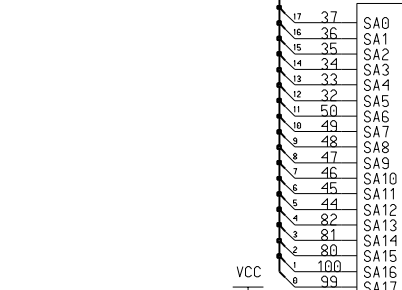
MEM_DATA1(8:0)

MEM_DATAH(8:0)

MEM_ADDR(17:0)

U64
MCM69P819

U67
MCM69P819



place 1 cap at each vcc pin

Engineer: H. Niggli	LBNL 1 CYCLOTRON ROAD BERKELEY, CA 94720	
Drawn by: H. Niggli	TITLE: 2x18x256k BANK OF SRAM	Size D
R&D CHK:		
DOC CTRL CHK:		
MFG CTRL CHK:		