Investigation of Oscillations in US Modules

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Introduction

This note reports our investigations into the oscillations observed in about 50% of the modules produced at LBL and to some extent at other sites. They occur in the noise occupancy scan as a deviation from the smooth error function (scurves) that is expected as the threshold is scanned from below zero to well above zero. During this test the chip is run in the level-latching mode (as opposed the edge latching mode) so that one expects 100% occupancy below thresholds where the interval between noise hits is much less than the length of the discriminator pulse. It is noteworthy that the problem only occurs on the backside of a module and, with one exception, is not seen on the hybrid before it is mounted on the module. First we will summarize our conclusions and report on the few successes we have had in reducing the oscillations and then we will describe a variety of test performed around parameters that seem to be uncorrelated with the effect.

Summary

On the basis of the tests described below we think the oscillations are due to feedback from the discriminator to the front end when a large number of channels make a transition in the same time bucket. The number of transitions required varies from chip to chip and depends upon the location of the chip on the hybrid but it ranges from 10% to 50% and consequently is not likely to be a problem in the normal running of the experiment. In addition we show that when the input charge is 1 fC no oscillation is present (Fig. 1c).

The most revealing test we have made is to show that the oscillations disappear when every other chip is turned off by reducing the front-end bias current and the shaping current to zero. Fig. 2a and Fig. 2b show the occupancy curves for the six chips on the backside (link 1) of a module and the scurves with every other chip off. The oscillations are clearly visible in fig. 2a and not in fig. 2b. This indicates that this is a regenerative effect involving many channels. To explore this avenue further we performed a series of tests on the same module using the trim to deliberately separate channel thresholds in an attempt to change the number of discriminator transitions at any given threshold.

A test consisting of displacing the thresholds of every other chip (Fig. 3a) shows the same effect on the oscillations (no oscillation) as turning off every other chip. By displacing the threshold every other channel we also see no oscillation (fig. 3b) showing that the number of channels is more important than the geometric arrangement of the channels.

Status

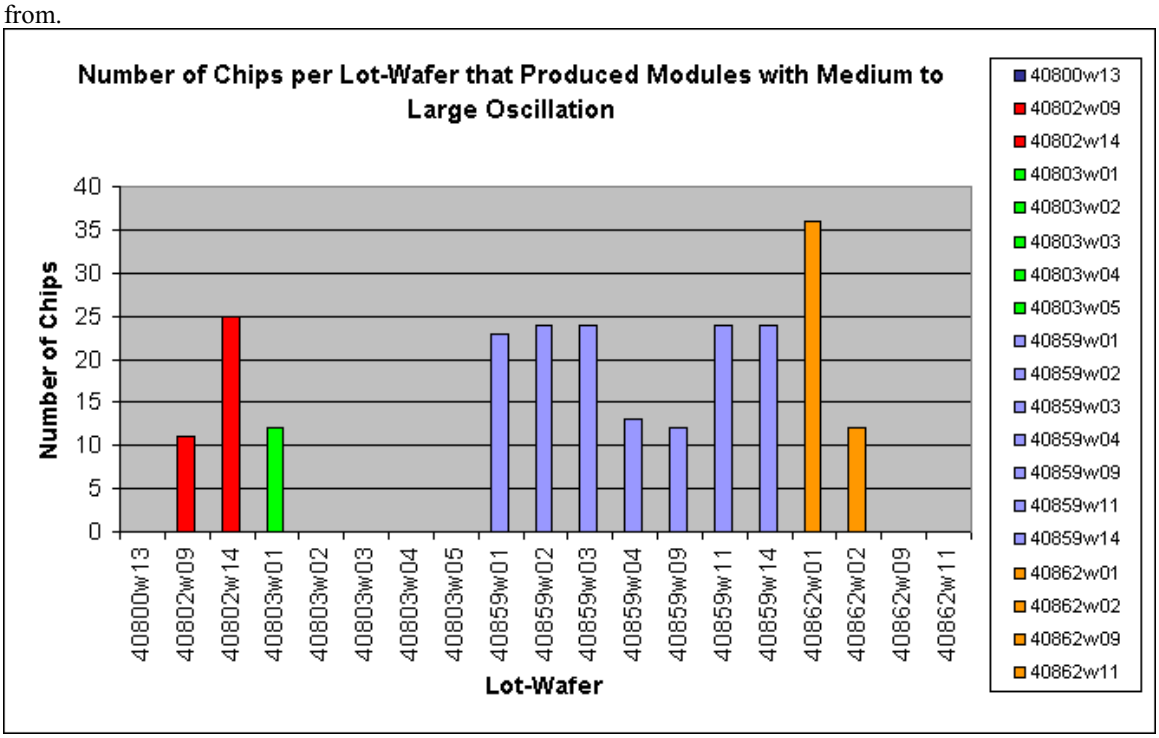
A total of 40 modules have been analyzed for oscillation. The complete summary of the tests performed including links to NO/Scurve plots from tests at 0 ^{o}C and at room temperature (and for 0.5, 1 fC injected charge) can be found at:
http://www-atlas.lbl.gov/strips/modules/production/analysis/NOcc/NO_Oscill_studies.xls

The following table summarizes the level of oscillation per module at 0 ^{o}C.

Hybrid	Module	Oscillation at 0 °C and no charge	Chips #
20220040200008	P02	large	7, 8, 9, 10,11
20220040200010	P03	minimal	7, 9
20220040200009	P04	medium	7, 8, 9, 10,11
20220040200011	P06	minimal	1
20220040200012	P07	none	none
20220040200014	P08	none	none
20220040200016	P09	none	none
20220040200017	P10	large	6, 7, 8, 9, 10, 11
20220040200018	P11	large	6, 7, 8, 9, 10, 11
20220040200019	P12	minimal	3, 7, 9, 10, 11
20220040200023	P13	medium	7, 8, 9, 10,11
20220040200015	P14	minimal	5
20220040200020	P15	medium	0, 5, 6, 7, 8, 9, 10, 11
20220040200037	P16	minimal	0-5, 6-11
20220040200038	P17	none	none
20220040200028	P18	medium	7, 8, 9, 10,11
20220040200040	P19	none	none
20220040200024	P20	minimal	7, 9, 11
20220040200041	P23	minimal	0, 1, 2, 3, 5-11
20220040200025	P24	none	none
20220040200042	P27	minimal	3
20220040200030	P28	large	7, 8, 9, 10,11
20220040200032	P29	medium	4, 6, 7, 8, 9, 10, 11
20220040200043	P31	large	6, 7, 8, 9, 10, 11
20220040200027	P32	medium	0, 1, 2, 3, 5-11
20220040200044	P33	large	0-5, 6-11
20220040200069	P34	large	6, 7, 8, 9, 10, 11
20220040200045	P35	large	7, 8, 9, 10, 11
20220040200049	P36	none	none
20220040200051	P37	minimal	11
20220040200033	P38	large	0-5, 6-11
20220040200061	P39	large	0-5, 6-11
20220040200034	P40	large	0-5, 6-11
20220040200053	P41	none	none
20220040200036	P42	minimal	6, 7, 8, 9, 10, 11
20220040200063	P44	large	3, 4, 5, 6, 7, 8, 9, 10, 11
20220040200062	P46	large	6, 7, 8, 9, 10, 11
20220040200065	P47	medium	7, 8, 9, 10, 11
20220040200070	P48	medium	4, 5, 8, 9, 10, 11
20220040200071	P53	medium	6, 7, 8, 9, 10, 11

At 0 °C (after a longterm test) 22 modules show large/medium oscillation, 10 minimal and 8 none. The oscillations decrease slightly at room temperature (see plots in the excel summary file). Large wiggles are mostly present for chips on the bottom of the module, and when there oscillations on the top of the module those wiggles they are usually very small.
Scurves of the same hybrids used in these modules show no oscillation at the hybrid level except in one case, Hybrid ID 20220040200018, where 2 chips show oscillation also at the hybrid level.

The hydrid summary (and plots) can be found in a sheet (Hybrid Study) in the same summary spreadsheet mentioned above. The total number of oscillation cases found in hybrids is 8 out of 85 hybrids analyzed and they involve isolated chips (unlike the modules where, for the most part, the oscillations are on the last chips).
The information of the Lot ID for the hybrids used is also given in the main summary excel file.
No correlation is particularly evident based on this list.
Wafer lots used are also indicated in the same summary file.
Below is a table showing the number of chips that show oscillation on modules versus the wafer they come from.



The table below summarizes the average of the level of oscillation found in the lot used, using a scale from 1 (none) to 4 (large) as seen in the scurves. The statistics are not very significant since most of the chips come from one particular lot, but it is true that modules with chips from lot Z40802 are all oscillating.

Lot #	#of modules	# of Wafers	Oscillation (average)	%modules with oscillation
Z40859	23	7	2.57	72
Z40800	2	1	1.50	50
Z40802	5	2	3.20	100
Z40862	7	4	2.71	71
Z40803	3	2	3.00	67

Charge Injection

The scurves also show wiggles at 0.5 fC injected charge when the oscillation is large in the NOcc scan. The wiggling usually disappears when the injected charge is 1fC and only very minor wiggles can be seen in a very few cases.
The following are 3 examples of scurves at no charge, 0.5 fC and 1 fC.

Figure 1a. Link 1 no charge.

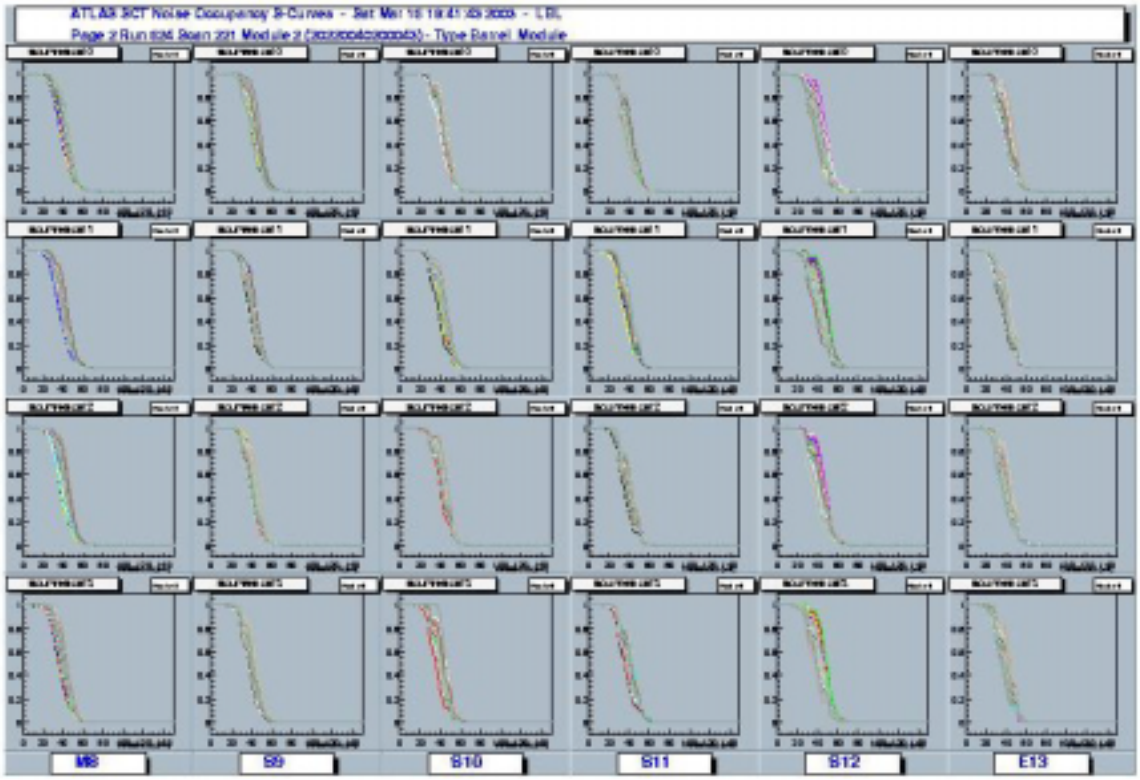


Figure 1b. Link1 0.5 fC charge

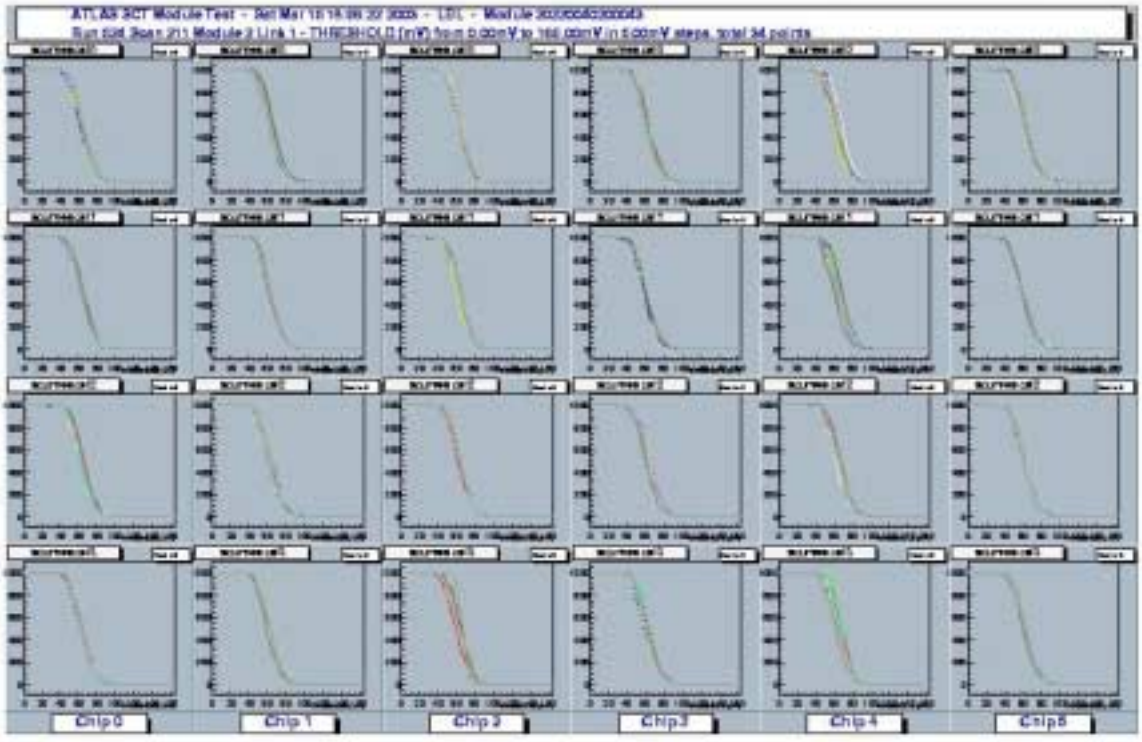
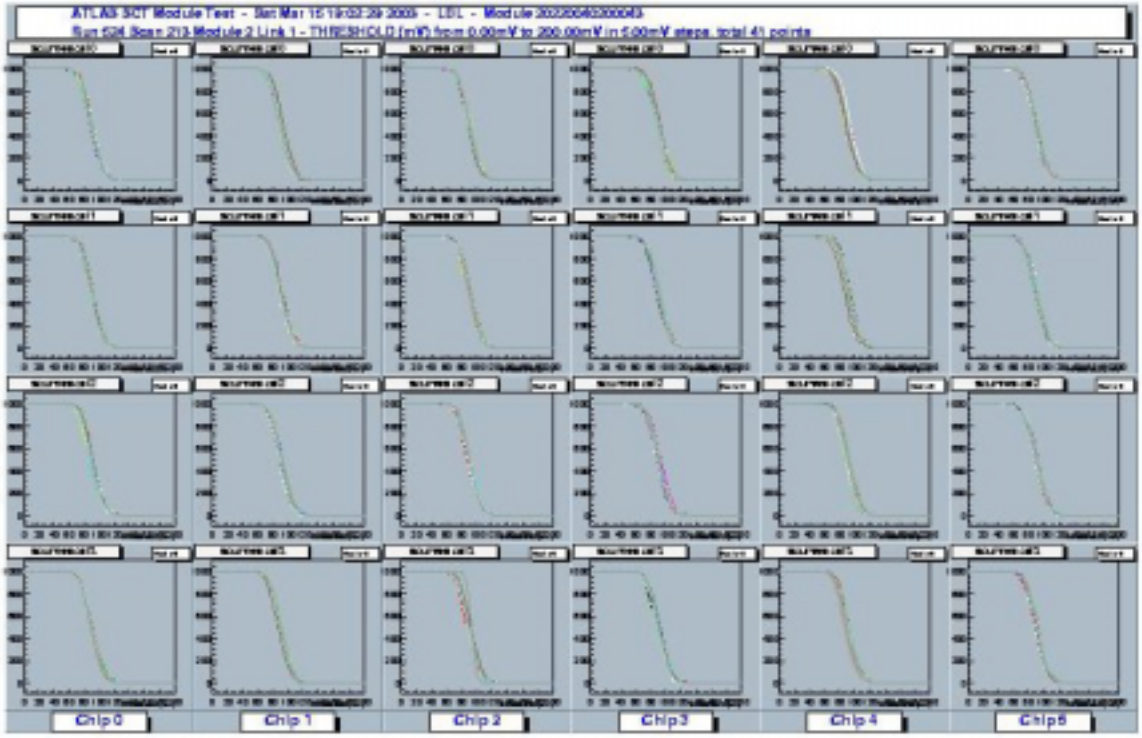


Figure 1c. Link1 with 1fC charge



Tests of FE currents/voltage settings

For modules 20220040200017 and 20220040200043 (at room temperature) results are given below for Vcc=3.7 Vcc=3.9 and combinations of ISH and FEBias currents settings.
Higher Vcc settings don't seem to have any effect on the existing oscillation. It's still there. Setting ISH=20μA (FEBias nominal at 220 μA) reduces the oscillation significantly whereas at reduced FEBias (150 μA) and nominal ISH current the two modules still show oscillation.

Turning off every other chip (by reducing the Febias and ISH to zero) makes the oscillation disappear for the 6 active chips (Vcc and Vdd is applied to all). This is our most dramatic success.

Vary Vcc, ISH, FEBias						
		Vcc=3.7 V	Vcc=3.9 V	ISH=20 all chips	ISH=30 FEBias=150	every other chip
202240200017	warm	plots scurves	plots scurves	plots scurves	plots scurves	plots scurves
202240200043	warm	plots scurves	plots scurves	plots scurves	plots scurves	plots scurves
	Results:	oscillation	oscillation	reduced oscillation	OSCILLATION (slightly reduced)	No oscillation

For 00033 and 00061 (at 0 °C) various runs with a few chips at the time ON were performed. Starting with M0, M8 and E13 ON, while ISH=0 and FEBias=0 for the others (Vcc, Vdd applied to all) and adding S12, then S11 all the scurves for these chips are perfect, except in the case of 00033 where oscillation starts to reappear with the addition of S11.
A last run with every other chip ON shows perfect scurves in both cases (S11 is not present). A test of all the chips ON except S11 shows a much reduced oscillation overall. M8 + entire link 1 in both cases show oscillation on the entire link.

Study of power distribution and transient currents						
		CHIPS present (ISH=0 and FEBias =0 for the excluded chips) but Vcc and Vdd to all				
		M0, M8, E13	M0, M8,S12,E13	M0, M8, S11, S12, E13	M0, and all link1	every other chip
202240200033	0 °C	scurves NO plots	scurves NO plots	scurves NO plots	scurves NO plots	scurves NO plots
202240200061	0 °C	scurves NO plots	scurves NO plots	scurves NO plots	scurves NO plots	scurves NO plots
	Results:	No oscillation	No oscillation	No oscillation on 00061 but YES on 00033	OSCILLATION	No oscillation
		M0, M8, S10, S12, E13	M0, M8, S11, S12,E13	M0, M8, S9, S10, S12, E13		link0 and all link1 except S11
202240200033	warm	scurves NO plots	Scurves NO plots	scurves NO plots		scurves NO plots
	Results:	No oscillation	Oscillaton on last 3 chips	No oscillation when excluding S11		All chips except S11 introduces a small oscillation on the last chips

From all of the above tests, the most revealing is the one showing that the oscillations disappear when every other chip is turned off (by reducing the front end bias current and the shaping current to zero). Fig.2a shows the occupancy curves for the six chips on the backside (link 1) of module 033 and Fig.2b shows the scurves with every other chip off. The oscillations are clearly visible in fig. 2a and not in fig. 2b.

Figure 2a. Module 20220040200033 link1. M0 + link1 are ON.

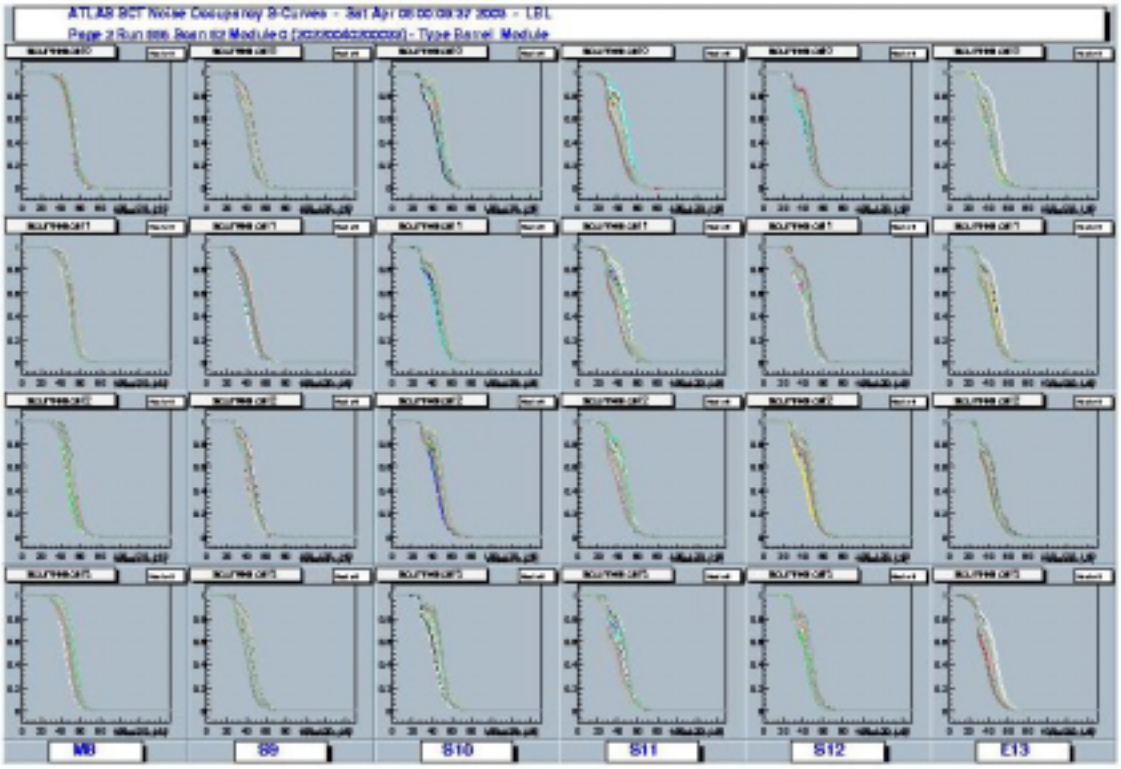
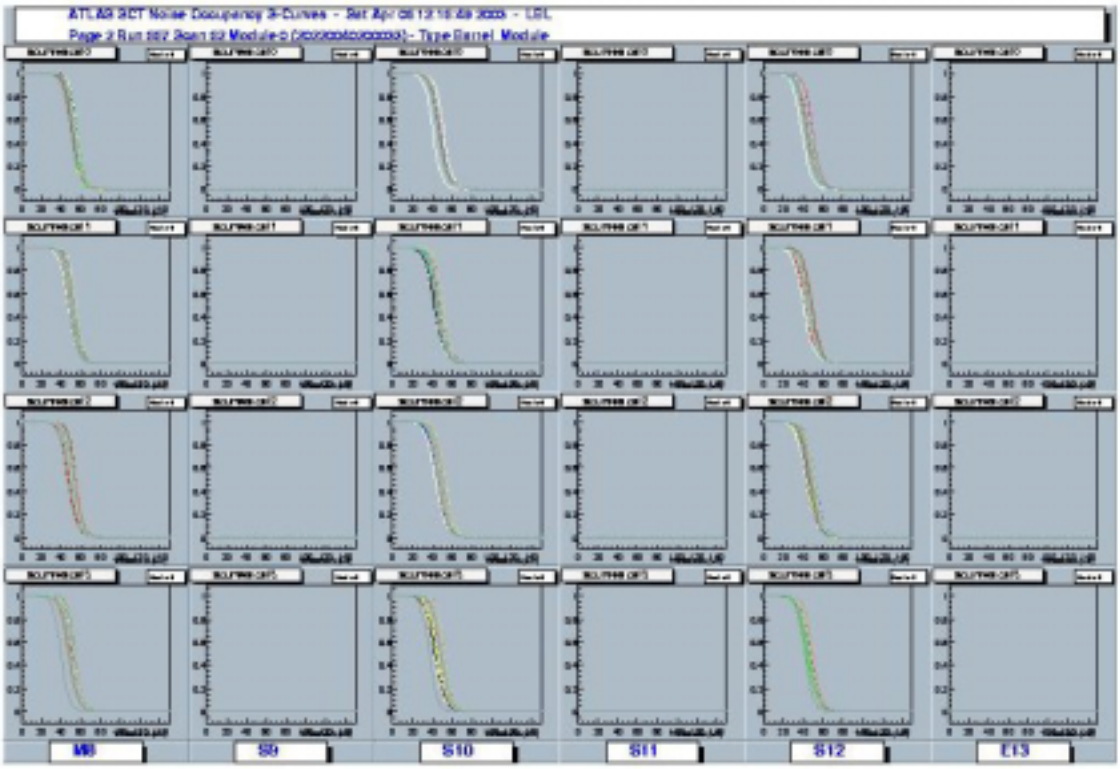


Figure 2b. Module 20220040200033 link1. Every other chip is ON.



Threshold study

We performed a series of tests on module 202240200033 using the trim to deliberately separate channel thresholds in an attempt to change the number of discriminator transitions at any given threshold. The following table shows the list of tests that we performed.

1	TRIM RANGE Standard Characterization	Scurves	NOPlots	Large Oscillation
2	TRIM RANGE 1 +1 unit (9mV) to Odd Channels	Scurves	NOPlots	Medium Oscillation
3	TRIM RANGE 1 +3 unit (27mV) to Odd CHIPS	Scurves	NOPlots	No Oscillation
4	TRIM RANGE 2	Scurves	NOPlots	Medium Oscillation
5	TRIM RANGE 2 +1 unit (12mV) to Odd Channels	Scurves	NOPlots	No Oscillation
6	TRIM RANGE 2 +4 unit (48mV) to Odd Channels	Scurves	NOPlots	No Oscillation
7	TRIM VALUE 8	Scurves	NOPlots	No Oscillation

Test 3 shows that displacing the thresholds of every other chip has the same effect on the oscillations as turning off every other chip. Tests 5 and 6 show that the number of channels is more important than the geometric arrangement of the channels.

Figure 3a. Module20220040200033 TRIM RANGE 1 +3 unit (27mV) to Odd CHIPS

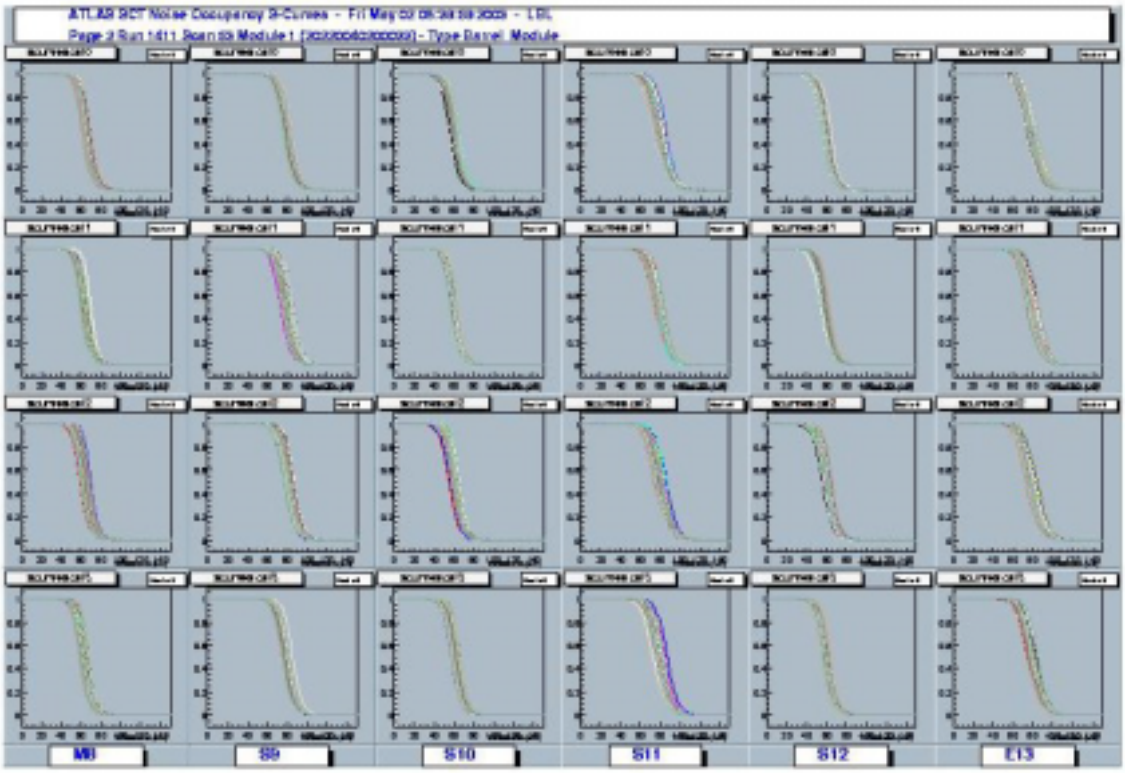
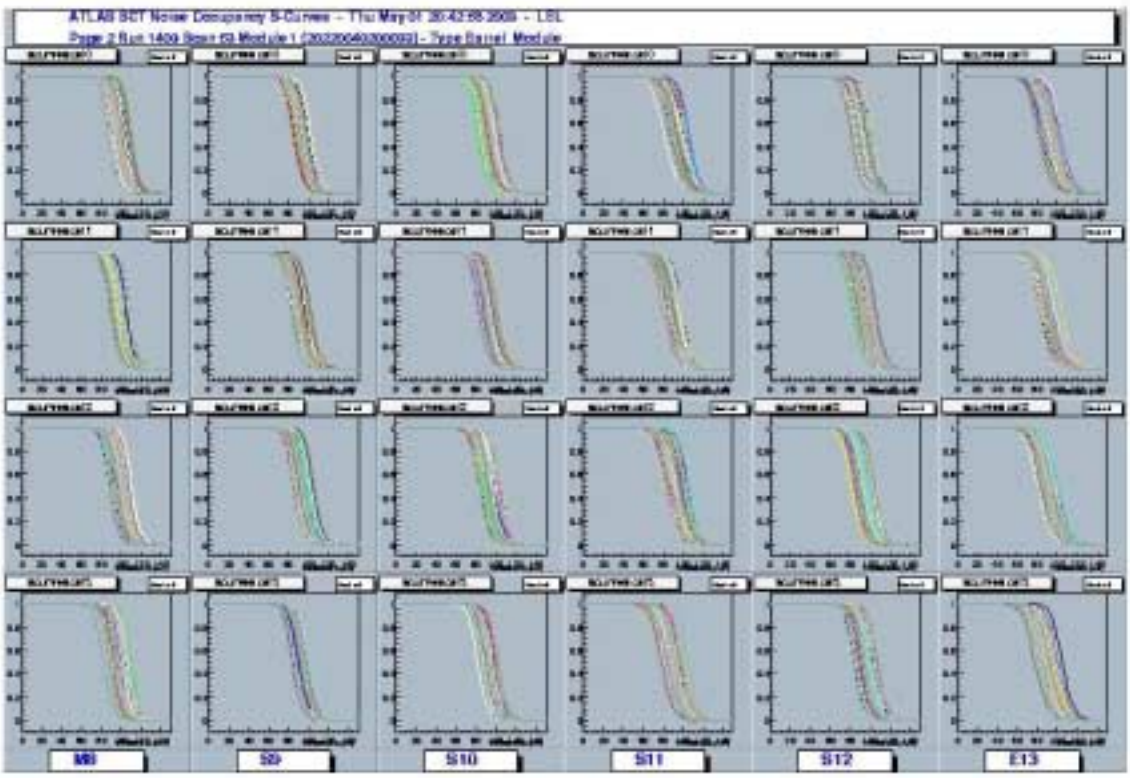


Figure 3b. Module20220040200033 TRIM RANGE 2 +1 unit (12mV) to Odd Channels



Grounding Scheme

The Grounding scheme has been re-checked and further tests have been performed to study various effects.

DAQ

The DAQ system comprises the basic modules but we don't use the CLOAC.

To reduce or eliminate possible sources of pick up noise we use:

- An external filter circuit based on Ned's designs for PP3
- A power cable made from screened twisted pair with an extra-screened twisted pair rated to 600V for the detector bias. The two cables are strapped tightly together and their screens are linked at both ends. The cable is 4m long. The power cable screens are connected together at each end of the cable and connected to the SCREEN pin of the connector (pin 18). There is a jumper on SCTLV3 to connect this pin to VME ground or through a capacitor (jumper J31/J41). We use the DC connection as it is used in the UK.

An earlier version of our cables was connecting the screen only at the VME side (not at the module side to avoid ground loops). But one cable was recently modified to connect the cables screens at both ends and then to pin 18. No difference was found with this new (UK) scheme.

AG

ANGD and DGND from module go to the module metal box through patch card screw holes (they have a metal ring connected to a trace on the card going to AG connector pins) that are in contact with the box

To prove the effectiveness of this connection we used non-conductive (rubber) washers instead of the metal ones normally used to make a better connection to ground. That showed that external noise is coupling into the normal noise giving a bad Noise Occupancy result (2 order of magnitude worse).

NO plots Scurves

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- We use the patch card from Scandinavian design. Cards were fabricated at CERN (through Lars) and then here in California based on the design by Olhe. UK fabricated theirs, Nobu his. This could be an issue if UK or Japan produced their cards changing the design.
- Subsequent information received from Nobu on how he has modified his card to improve the ground connection to the box (ANGD pins are soldered to copper tape in contact with screws to the metal box), led to an additional test, which consisted, on modifying similarly our card. A test of a module using this scheme showed a very similar level of oscillation.
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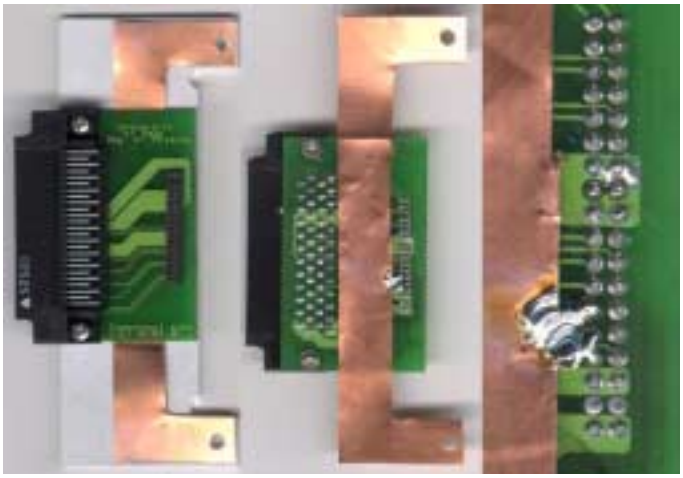
Patch card modifications



Power distribution.

In order to improve the power distribution to bottom side of the module, cables were soldered to the low frequency capacitors connecting from the patch card Vcc, Vdd, and Ground.
No difference on the oscillation level was observed.

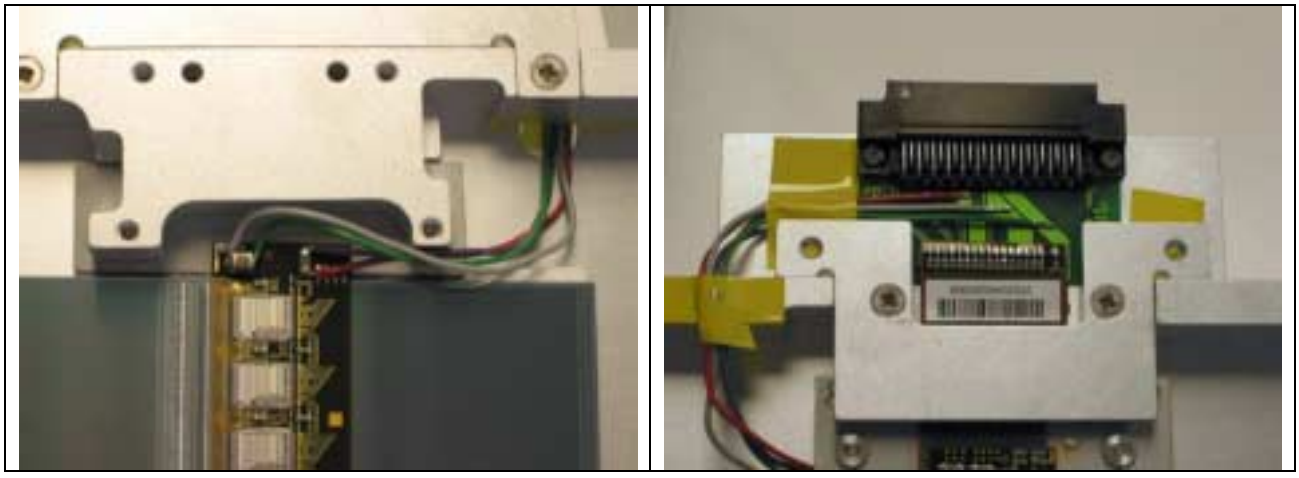
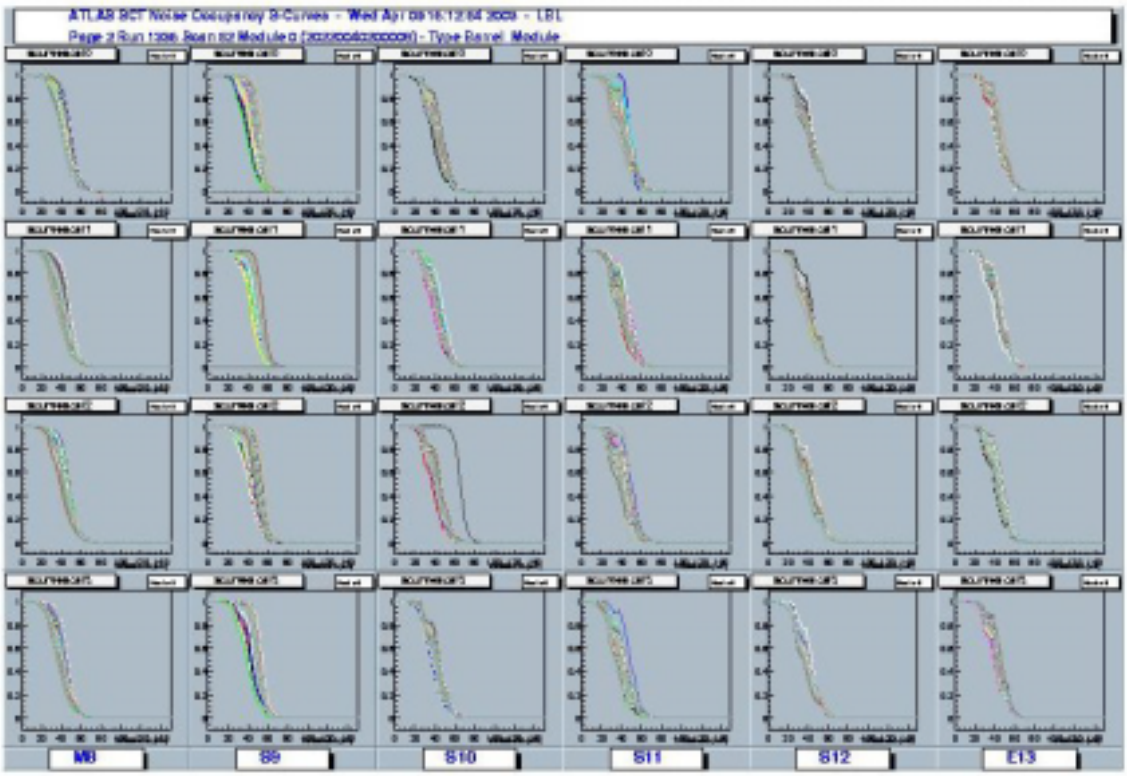


Figure 4. Module 20220040200008 link1 after power distribution modification



Quantification of the oscillation (Abe's plot).

The standard plots produced with the NO occupancy test include the analysis fit of ln(occ) vs thr^2 to estimate the equivalent noise charge. One can see that the fit for thresholds above 0.5fc is always good even in the case of modules that show large oscillation, while typically in the region around and below 0.5 fC (blue data points) is where the oscillation occurs (if present and in that case the no-fitted region is not smooth, it is either curved or segmented). By going down to zero threshold there are two classes of behavior:

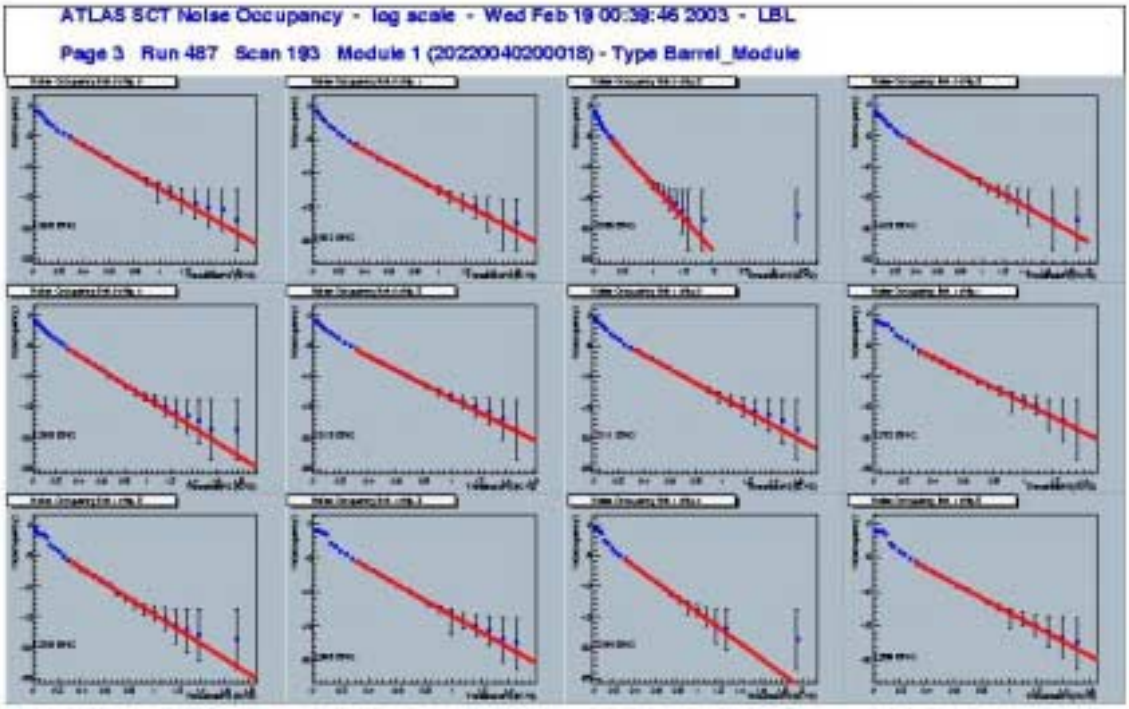
1) A smooth rise in occupancy above the straight line as the threshold is lowered for thresholds below 0.5fC (square). These give the smooth S-curves

2) A number of modules which follow the straight line behavior down to lower threshold and then jump up to higher occupancy. These show the wiggly S-curves. The jump is typically around 0.35 fC.

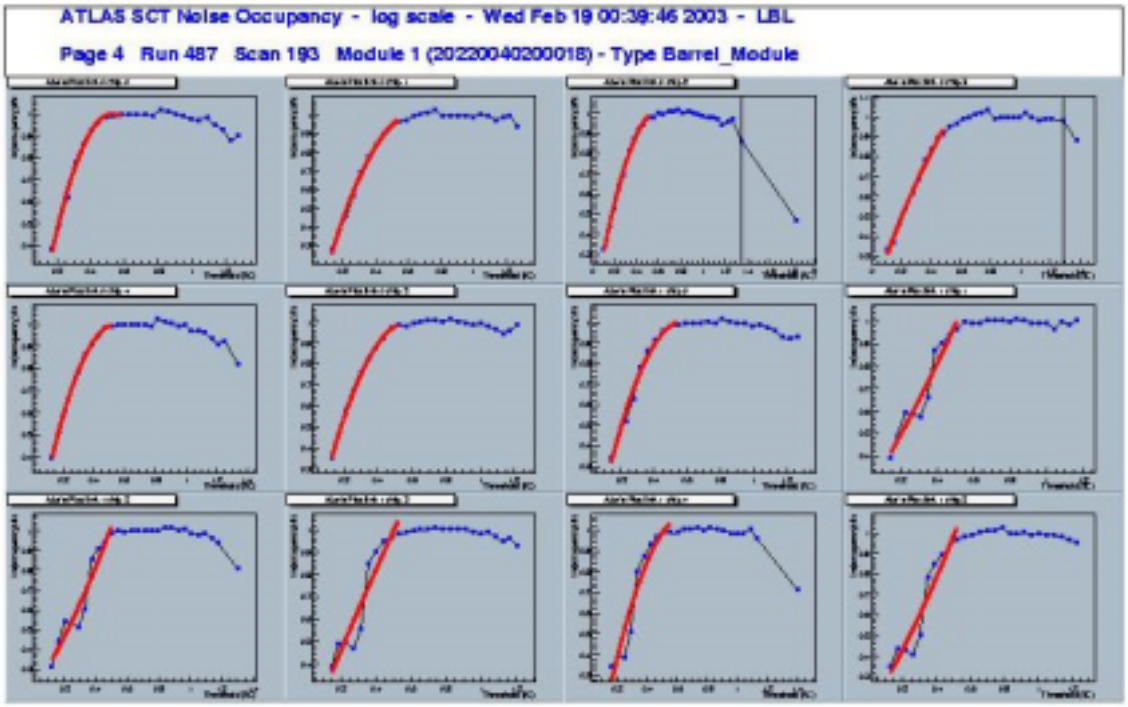
In order to have a quantitative measure of the wiggles we produced a new set of plots (Abe's plot) where the data is divided by the fit values and it is plotted as the ln(Occ) vs Threshold (no square). We then fit the first 10 points of the ln(occ)/fit plot. The mean square deviation (var) is significantly larger for most of the chips with large 'wiggles'.

Below the two sets of plots per chip showing the standard plots and the Abe plot with the fit.

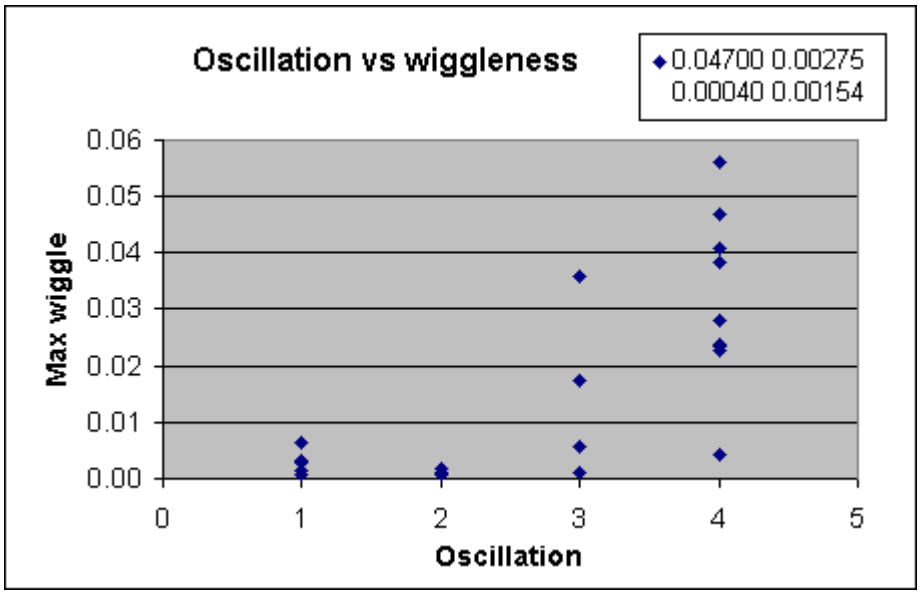
Standard fit.



Abe's plot

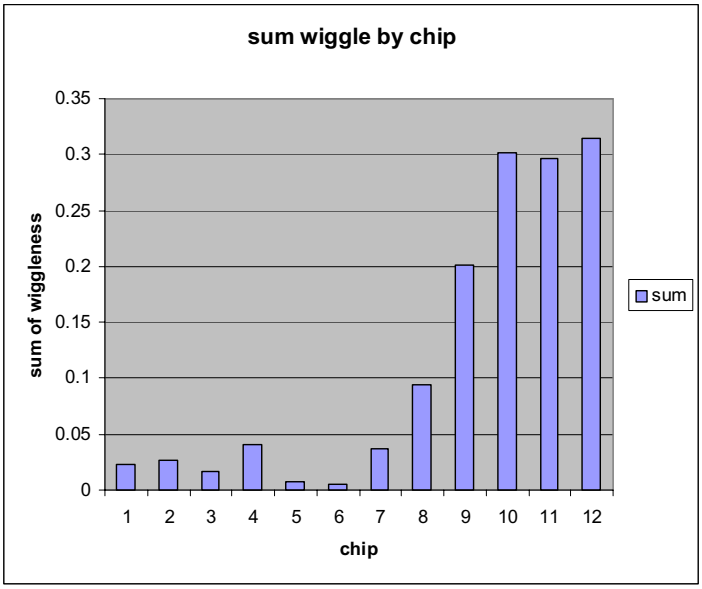


We classify (visually) the magnitude of the oscillations by module as large(4), medium(3), small(2) and none(1). The plot below shows the largest deviation in the module vs magnitude of oscillation (the fit was done chip by chip). Clearly the correlation is high and a cut of .01 identifies all but three of the large and medium cases.



The plot below is a bar plot of the sum, for each position on the hybrid, of the mean square deviation for all of modules classified medium and large. It clearly shows that not only the problem is on the back side but it increases from small to large from chip 7 to chip 12. Obviously it is worst in last three or four chips of the hybrid.
Anomalous chips may contribute to the problem but they are only a problem at the end of the hybrid.

Sum of mean square deviation for modules with oscillation by chip



Gain and Speed correlation studies.

A comprehensive analysis has been carried on to study possible correlations between chips behavior at wafer, hybrid and module level and their oscillation. A detailed list of histograms showing gain, gain RMS, TW, Strobe Delay distributions by grouping chips on stream0 and chips on stream1 (since the oscillation is mainly present in the Bottom of the modules) and for wafer, hybrid and module can be found at:

http://www-atlas.lbl.gov/strips/modules/production/analysis/NOcc/

A README file describing how to interpret the various histograms can be found in the same page.
List of the histograms available:

1-D histograms
grms.ps: Gain RMS and Gain distributions.
speed.ps: Timewalk and Strobe Delay distributions.

2-D histograms
gsd.ps: Strobe Delay vs. Gain.
gtw.ps: Timewalk vs. Gain
grmssd.ps: Strobe Delay vs. Gain RMS
grmstw.ps: Timewalk vs. Gain RMS
sdtw.ps: Timewalk vs. Strobe Delay

No correlation to oscillation has been found.

Conclusion.

- Modules where tested in multiple combinations of active chips showing that oscillation disappears (or is significantly reduced) when switching activity is reduced by isolating every other chip or excluding only one chip in a particular case, and setting the shaper current much lower than the nominal value (ISH=20). This indicates that this is a regenerative effect involving many channels.

- Further tests using the trim to deliberately separate channel thresholds in an attempt to change the number of discriminator transitions at any given threshold have shown that displacing the thresholds of every other chip has the same effect on the oscillations as turning off every other chip. Displacing the threshold every other channel demonstrated that the number of channels is more important than the geometric arrangement of the channels.

- No correlation was found with hybrid Lot

- We can't conclude that there is a correlation between modules with large oscillation and a particular Wafer Lot since we don't have enough statistics

- We introduced a method to quantify the oscillation (Abe's plot) where we fit the region of low threshold (the first 10 points of the ln(occ) plot). By looking at the mean square deviation of the fit (which is significantly larger for most of the chips with large wiggles) we can identify all but three cases of oscillation.

- No correlation was found between modules that show oscillation and oscillation at the hybrids level (except for one case, oscillation is not seen on the hybrid before it is mounted on the module that shows oscillation)

- There is no evidence of correlation between oscillating chips and gain, gain RMS, TW and Strobe delay (for same chips on modules, hybrids, wafer)

- The grounding scheme has been checked and we don't see evidence of pick up noise
    - We do see pick up noise when we tried to change the current scheme (we change connection to AGND)
    - Modules were tested at different stations - single module station, multiple module, in environmental chamber showing reproducible results
- Power was brought to the bottom of the module by connecting the low frequency capacitors from the patch card Vcc, Vdd, and Ground. No difference in the oscillation level was found.

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