ABCD Production Testing

- Example of a possible test procedure
- A custom ASIC tester

Example of a possible test procedure (I)

Power On Reset	• Turn on VDD to a minimum value and run a TV. Clk=40 MHz. Check if chip response is same as simulation result.
Power Consumption	• Set VDD to 4.0 V. Set VCC to 3.5 V. Set all DAC's to nominal values and chip into data taking mode. Measure Icc and Idd. Reject die if too high or too low.
Digital functionality, I/O Signal Amplitudes and Timing	• Run complete set of testvectors. Supply minimum amplitude signals with minimum setup time and latch output signals at maximum specified clk->out times and only if they cross the minimum specified amplitude threshold. Run testvectors at 3.6,4.0 and 4.4 V and at a minimum specified frequency (eg 55 MHz). Reject in case of one or more bit errors.

Example of a possible test procedure (II)

Preamplifier Current and Shaper Current DAC

- Scan through all possible values of the DACs and measure voltage on test pads. Reject die if one or more points outside a maximum allowed error band.

Front End Tests

- Set everything to nominal operating conditions. Take threshold scans (100 triggers for each point, 30 threshold settings) at 1.5 fC or so with all possible trim dac settings. Determine Gain, Noise and TrimDac Linearity. Acceptance criteria TBD.
- Measure one threshold scan at nominal settings, minimum/maximum shaper current and preamplifier current.
- Measure a Delay Scan at nominal settings.

Testing time with custom tester:

- 3s/chip including stepping (35% digital yield)

→ 12 min/wafer, now include 8 min alignment and handling

→ **24 wafers/day or 120 wafers/week**