V. Fadeyev, Apr 16'00

Test Vectors description courtesy F. Anghinolfi. Also shown are stimulated I/O lines. Each TV has the resetB input line de-asserted soon after the beginning (not indicated in this Table).

TV #	Stimulated Input Lines	Affected Output Lines	Purpose/Description
1	com0	datalink	Configuration register Write/Read test. Bits 0 thru 10 are scanned.
2	com0, id0, id1, id2, id3, id4	datalink	BC counter test (all 8 bits are checked). ID address bits test. Overflow function and error code test.
3	com0	datalink	Data Compression Logic tests with random channel mask. Having "one"s in different bits of the 3-bit hit discription.
4	com0, com1, select	datalink	Digital pipeline test. Accumulate function test with Com1/clock1 circuit.
5	com0, tokenin0, tokenin1, datain0, datain1	datalink, tokenout0, tokenout1, dataout0, dataout1	Data/tocken bypassing circuitry test.