Defective ASIC's

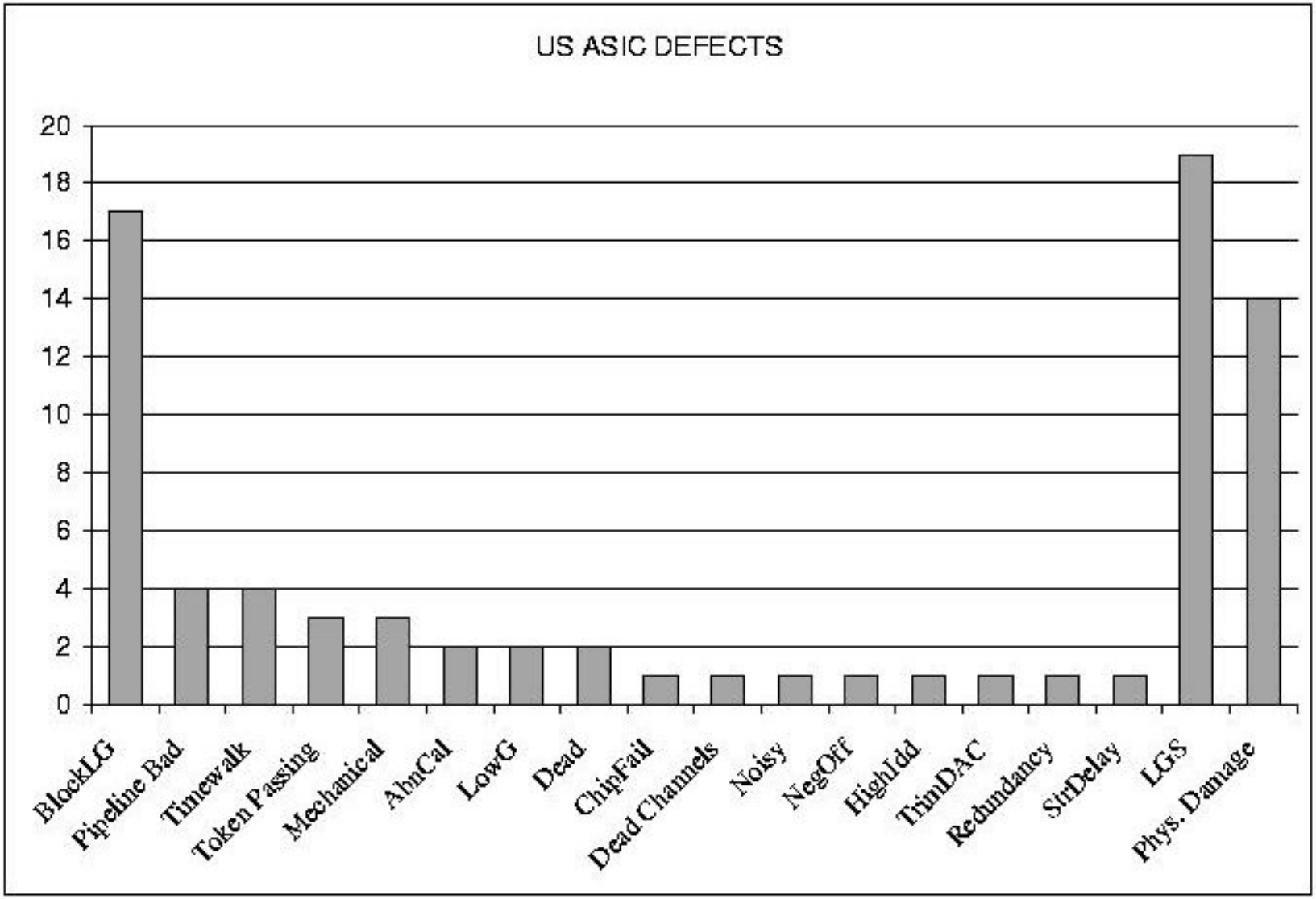
A. Ciocio - LBNL

List of Defective ASIC's

Hybrid Serial #	chip# on hybrid	lot/wafer	DEFECT	chip status
20220040200011	11	Z40859-W11	LGS	Replaced
20220040200013	6	Z40859-W02	Mechanical	Replaced
20220040200020	1	Z40859-W014	Token	Replaced
20220040200021	8	Z40859-W09	LGS	Replaced
20220040200021	7	Z40859-W09	BlockLG	HOLD
20220040200022	10	Z40859-W09	LowG	to rework
20220040200035	9	Z40859-W01	Mechanical	Replaced
20220040200035	6	Z40859-W01	TimeWalk	Replaced
20220040200039	10	Z40859-W04	Mechanical	Replaced
20220040200039	2	Z40859-W04	LGS	ok to use
20220040200039	6	Z40859-W04	LGS	ok to use
20220040200041	2	Z40802-W09	LGS	ok to use
20220040200046	9	Z40803-W02	LGS	ok to use
20220040200047	0	Z40862-W11	NegOff	to rework
20220040200048	6	Z40803-W02	AbnCal	ok to use
20220040200048	9	Z40803-W02	LGS	ok to use
20220040200050	10	Z40862-W11	TimeWalk	to rework
20220040200052	7	Z40862-W09	LGS	ok to use
20220040200054	4	Z40803-W05	LGS	ok to use
20220040200056	6	Z40803-W05	Highldd	Replaced
20220040200057	9	Z40862-W09	LGS	ok to use
20220040200058	7	Z40803-W05	TrimDAC	to rework
20220040200059	0	Z40803-W03	LowG	Replaced
20220040200064	0	Z40862-W02	Redundancy	to rework
20220040200068	1	Z40862-W02	LGS	ok to use
20220040200073	0	Z40803-W01	StrDelay	Replaced
20220040200098	6	Z41032-W13	BlockLG	HOLD
20220040200098	7	Z41032-W13	BlockLG	HOLD
20220040200099	0	Z41032-W13	BlockLG	HOLD
20220040200100	1	Z41032-W13	LGS	ok to use
20220040200100	7	Z41032-W13	BlockLG	HOLD
20220040200100	9	Z41032-W13	BlockLG	HOLD
20220040200107	8	Z41032-w12	BlockLG	HOLD
20220040200117	8	Z41032-w08	BlockLG	HOLD
20220040200119	0	Z41032-w08	Noisy	??done??
20220040200122	10	Z41032-w09	LGS	ok to use
20220040200128	3	Z40615-w19	Dead	HOLD
20220040200128	5	Z40615-w19	Timewalk	HOLD
20220040200132	7	Z41032-w08	Dead	??done??

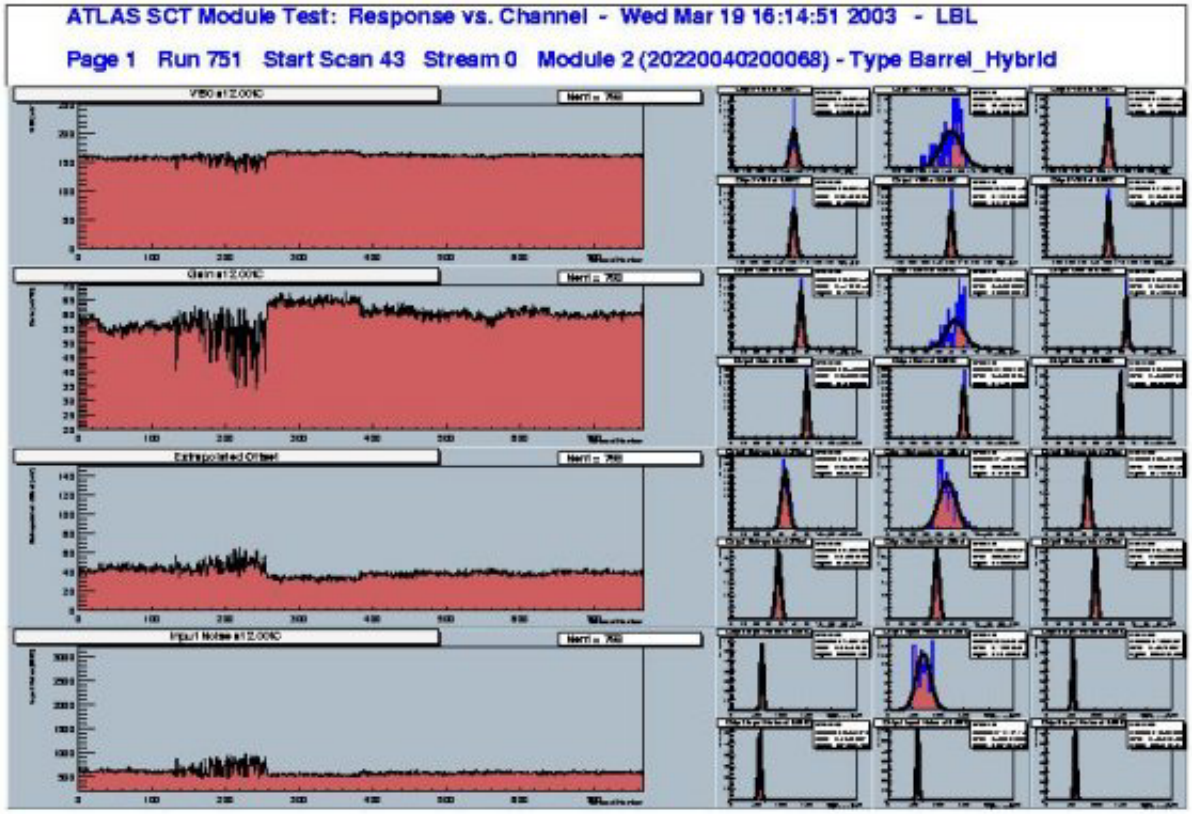
Hybrid Serial #	chip# on hybrid	lot/wafer	DEFECT	chip status
20220040200136	0	Z40803-W06	LGS	ok to use
20220040200137	9	Z40803-W06	LGS	ok to use
20220040200138	8	Z40803-W08	LGS	ok to use
20220040200141	0	Z40803-W08	LGS	ok to use
20220040200143	6	Z40920-W13	Chipfail	Replaced
20220040200144	2	Z40920-W15	AbnCal	Replaced
20220040200145	1	Z40920-W15	BlockLG	HOLD
20220040200148	6	Z41032-w12	BlockLG	HOLD
20220040200155	8	Z40920-W10	BlockLG	HOLD
20220040200156	4	Z40920-W10	BlockLG	HOLD
20220040200158	11	Z40920-W10	BlockLG	HOLD
20220040200160	8	Z41032-W13	BlockLG	HOLD
20220040200161	0	Z41032-W13	LGS	ok to use
20220040200164	9	Z41032-w17	Pipeline Bad	??done??
20220040200165	10	Z41032-w17	BlockLG	HOLD
20220040200165	8	Z41032-w17	BlockLG	HOLD
20220040200180	10	Z41032-w11	Pipeline Bad	to rework
20220040200180	10	Z41032-w11	Dead Channels	to rework
20220040200181	10	Z41032-w11	Physical Damage	HOLD
20220040200181	11	Z41032-w11	Physical Damage	HOLD
20220040200182	0	Z41032-w11	Physical Damage	Replaced
20220040200182	1	Z41032-w11	Physical Damage	Replaced
20220040200182	2	Z41032-w11	Physical Damage	Replaced
20220040200182	3	Z41032-w11	Physical Damage	Replaced
20220040200182	4	Z41032-w11	Physical Damage	Replaced
20220040200182	5	Z41032-w11	Physical Damage	Replaced
20220040200182	6	Z41032-w11	Physical Damage	Replaced
20220040200182	7	Z41032-w11	Physical Damage	Replaced
20220040200182	8	Z41032-w11	Physical Damage	Replaced
20220040200182	9	Z41032-w11	Physical Damage	Replaced
20220040200182	10	Z41032-w11	Physical Damage	Replaced
20220040200182	11	Z41032-w11	Physical Damage	Replaced
20220040200183	4	Z39693-W15	Pipeline Bad	Replaced
20220040200184	0	Z39693-w15	Pipeline Bad	??done??
20220040200185	8	Z39693-W15	Timewalk	Replaced
20220040200186	10	Z41032-w11	Token	Replaced
20220040200189	9	Z41032-w07	BlockLG	HOLD
20220040200192	3	Z39693-w15	Token	Replaced
20220040200193	11	Z39693-w15	LGS	ok to use

US ASIC's Defects



LGS

A study of the Large Gain Spread (LGS) effect was conducted in numerous ASIC's to better understand the causes, effects, and possible solutions

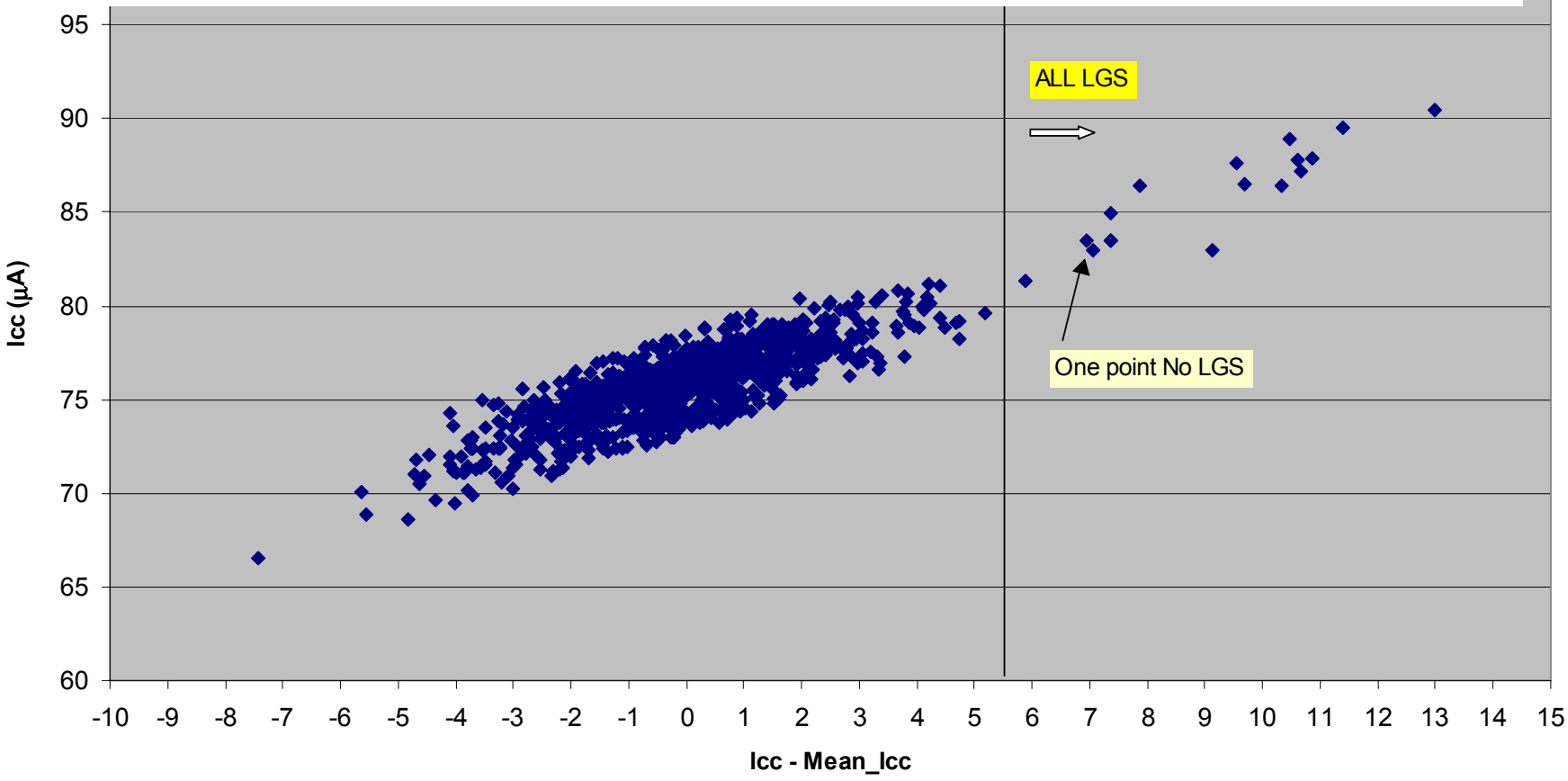


Areas of the Study

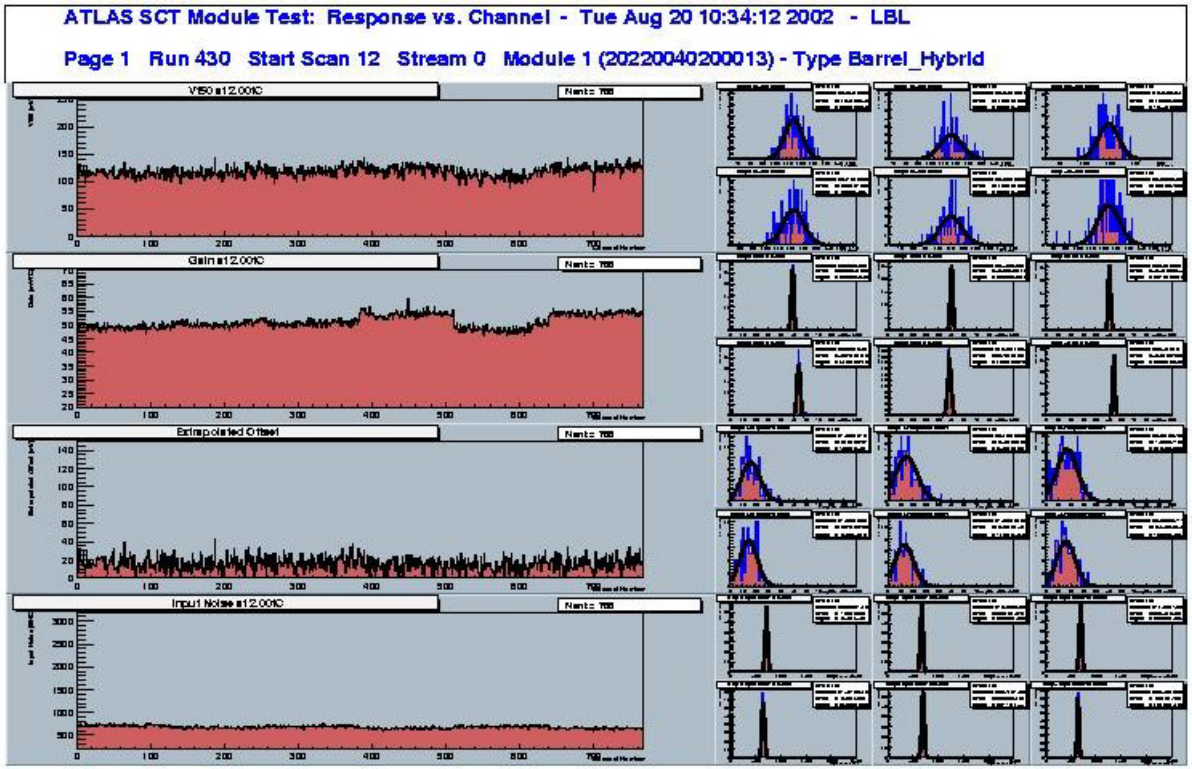
- ISh and Vcc
- Icc
- FE DAC's

Icc Study – Icc vs (Icc-mean) Correlation

Scatter plot of Icc versus the deviation of Icc from the mean Icc for each wafer (or gelpak) each chip is coming from All but one of the 17 chips with LGS can be identified by cutting at 5.5 (deviation from the mean Icc). This method can be used for pre-selecting chips before they are mounted on hybrids



Hybrid 20220040200013
Chip 2-5 Digital Tests Failure starting at 33°C



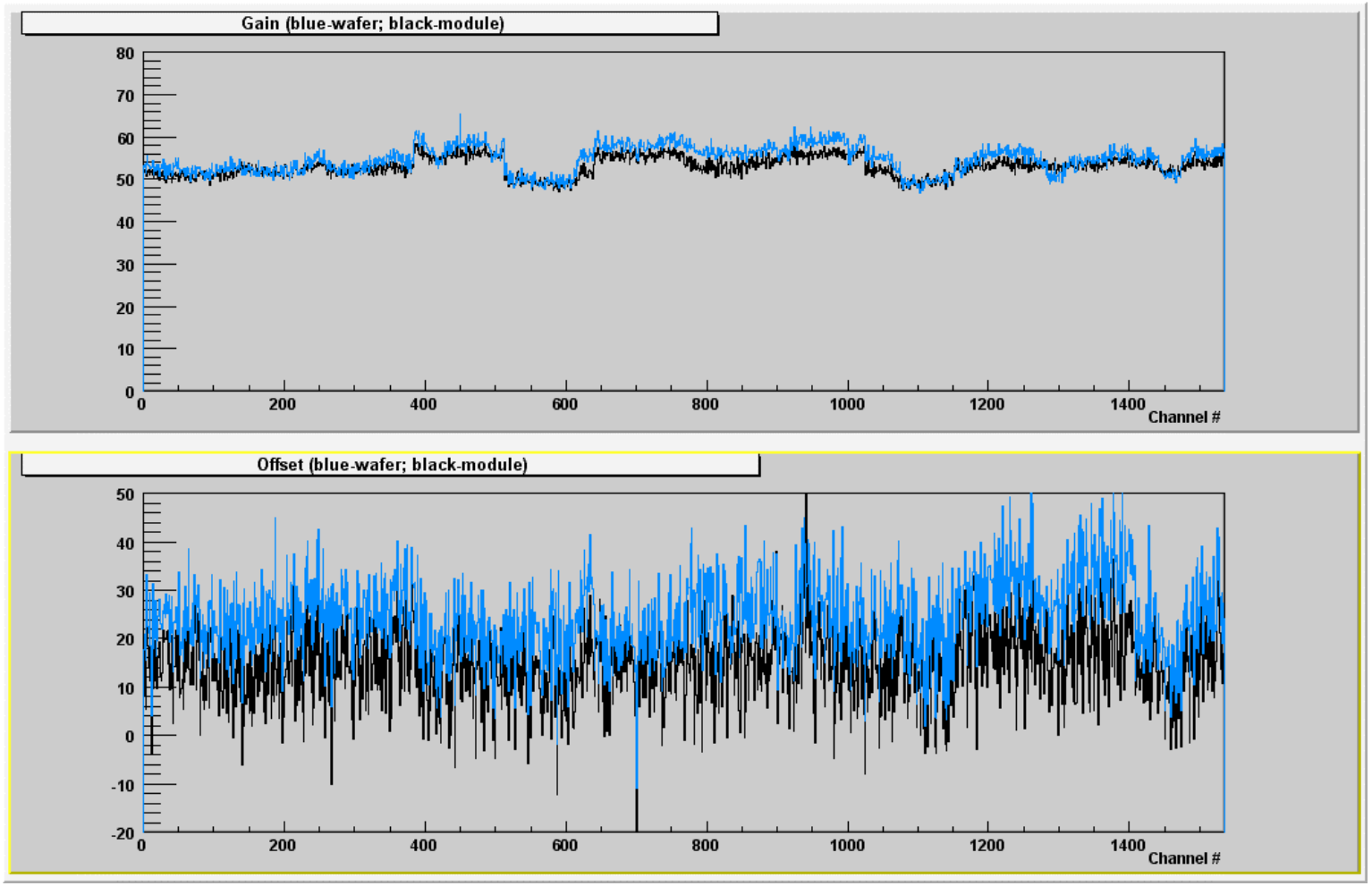
Three Point Gain Response at 37°C

Hybrid tests:
FullBypassTest: fails at Vdd = 3.5V but works fine at higher Vdd

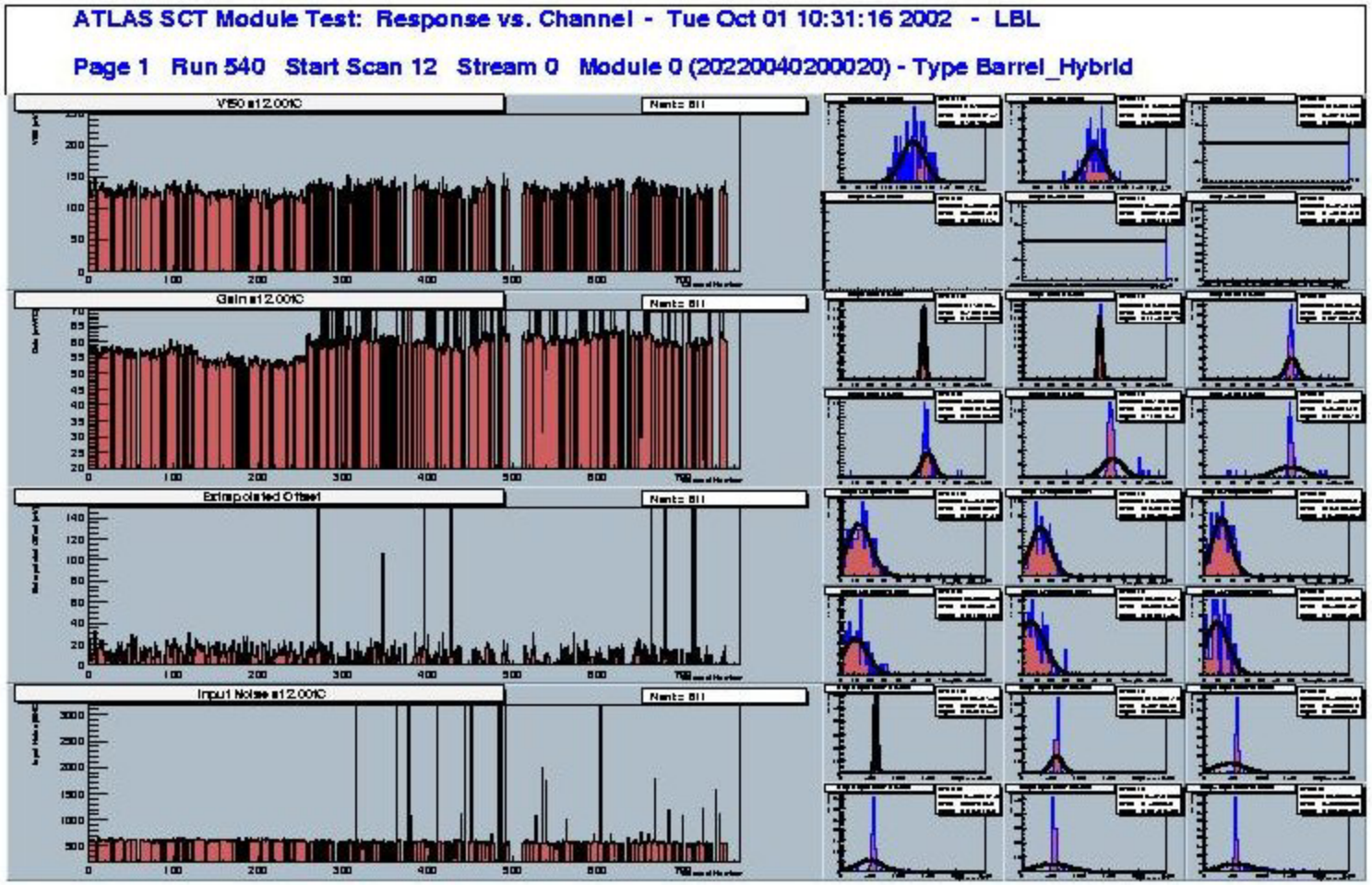
Wafer TV tests:
At 40 and 50 MHz all chips TV(eff) = 1 and all Vdd(eff) =1
except chip S02: at 50 MHz and Vdd=3.3V for TV2 to TV5 eff =0

The timing of the token passing is quite critical. At higher temperatures the CMOS is slower, so it could get closer to the edge.
It might be related to the quality of the clock signal.
It might work at a different system.

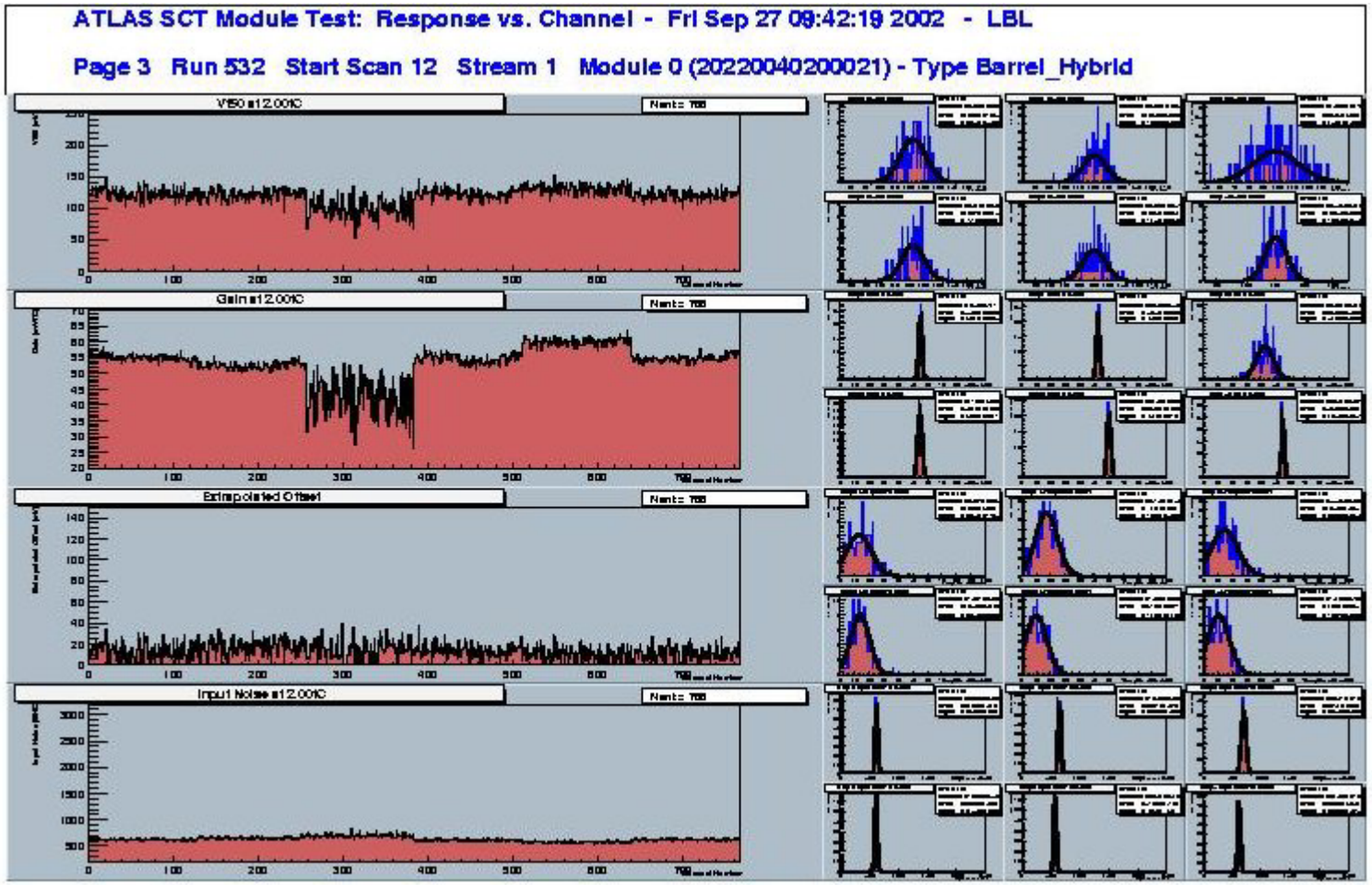
Hybrid 20220040200013
Wafer/Hybrid Comparison



Hybrid 20220040200020
chip 1 TOKEN Failure

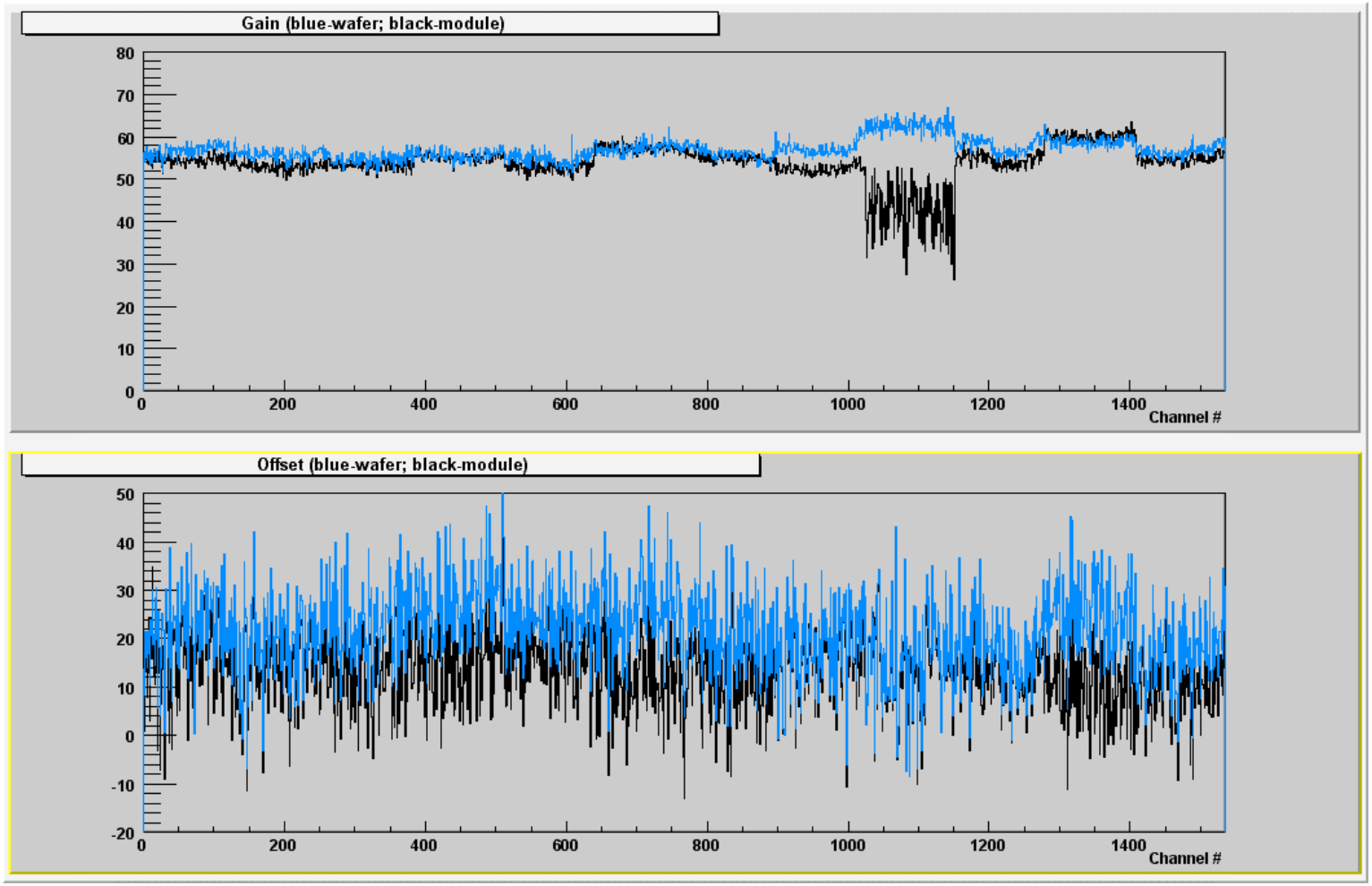


Hybrid 20220040200021
chip 8 Large Gain Spread

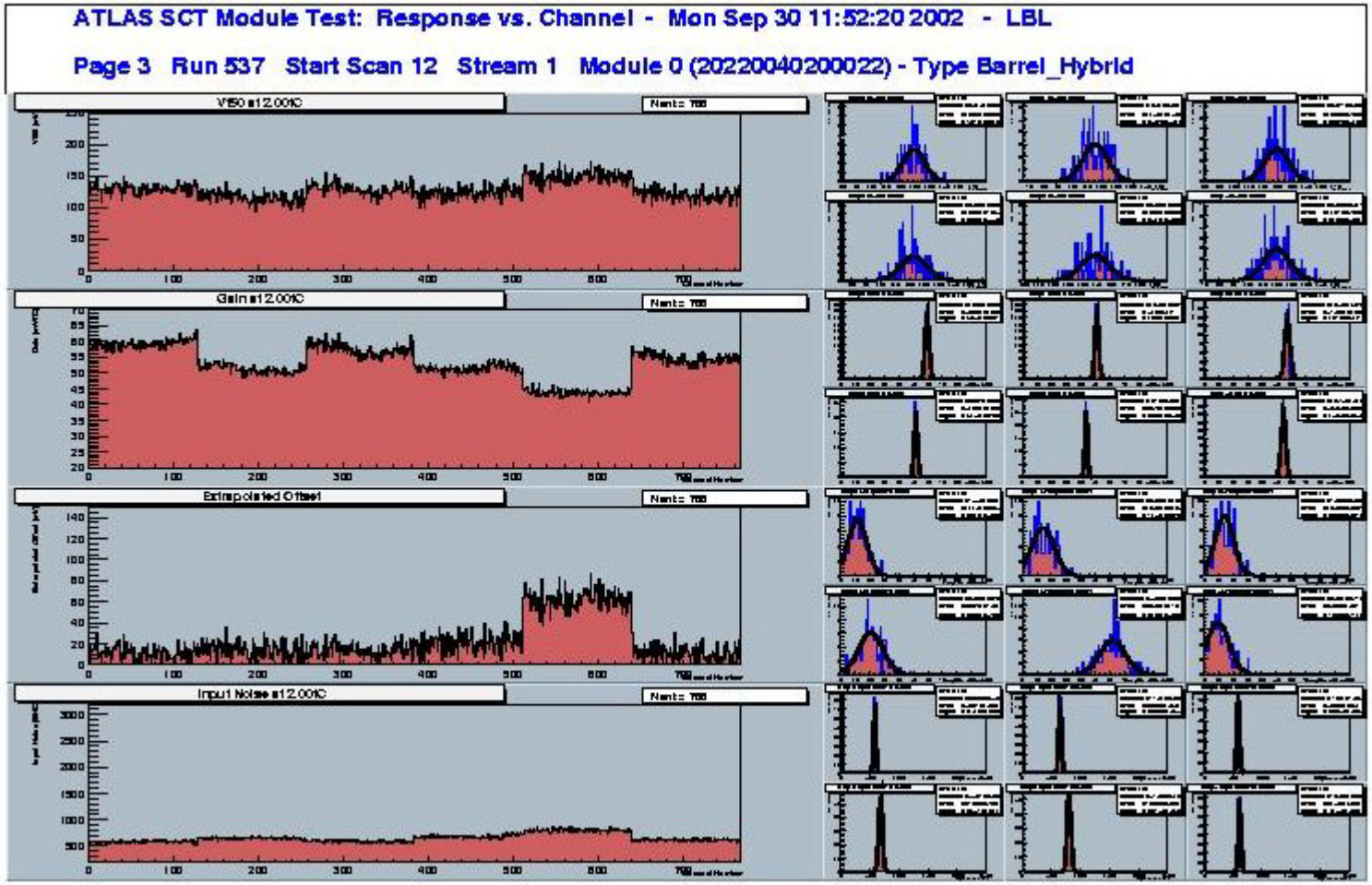


Chip started to work well at Vcc=3.7V - Voltage drop at the hybrid 50 mV
Under wafer test (test performed at UCSC) works at nominal Vcc

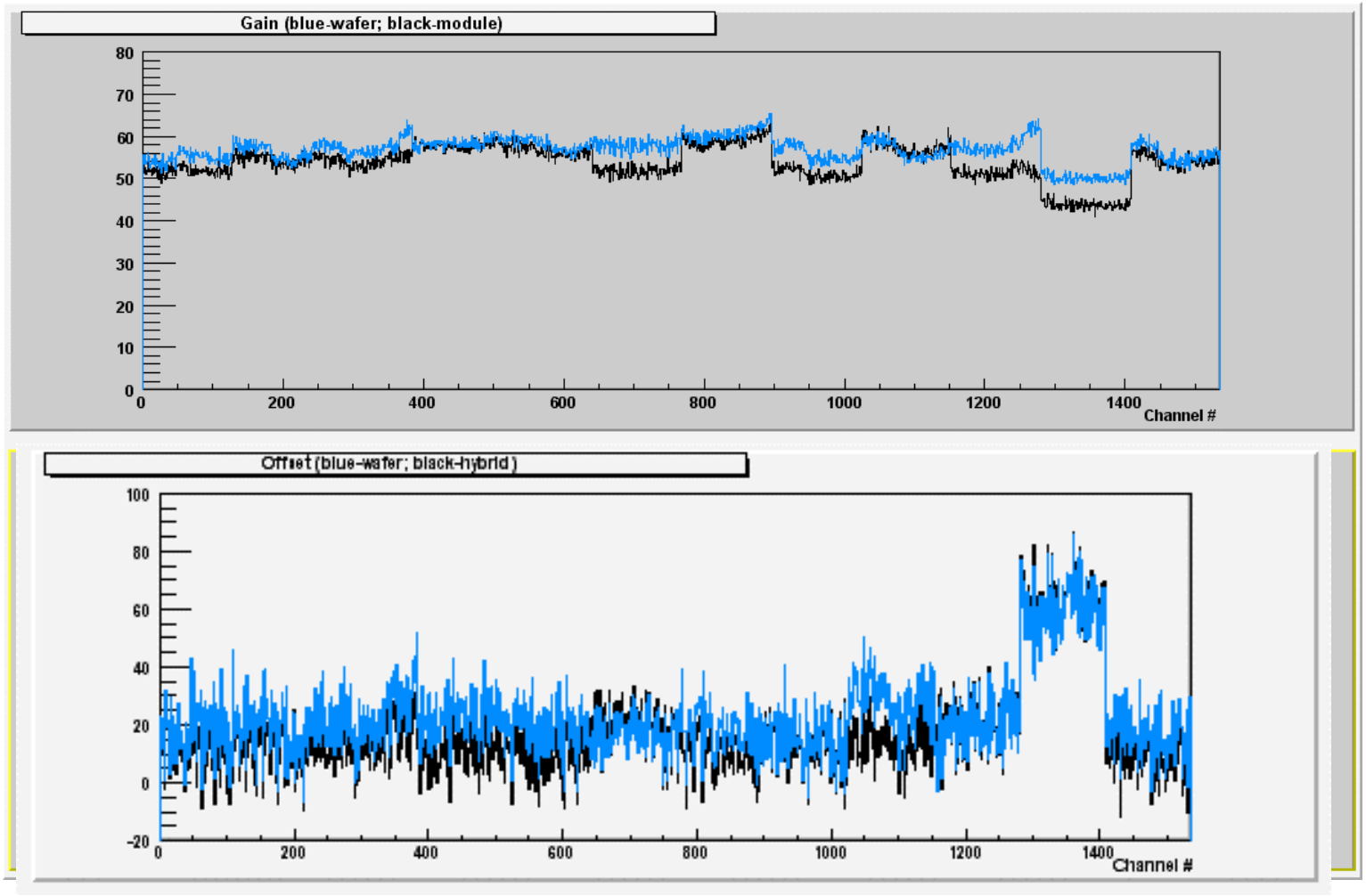
Hybrid 20220040200021
Wafer/Hybrid Comparison



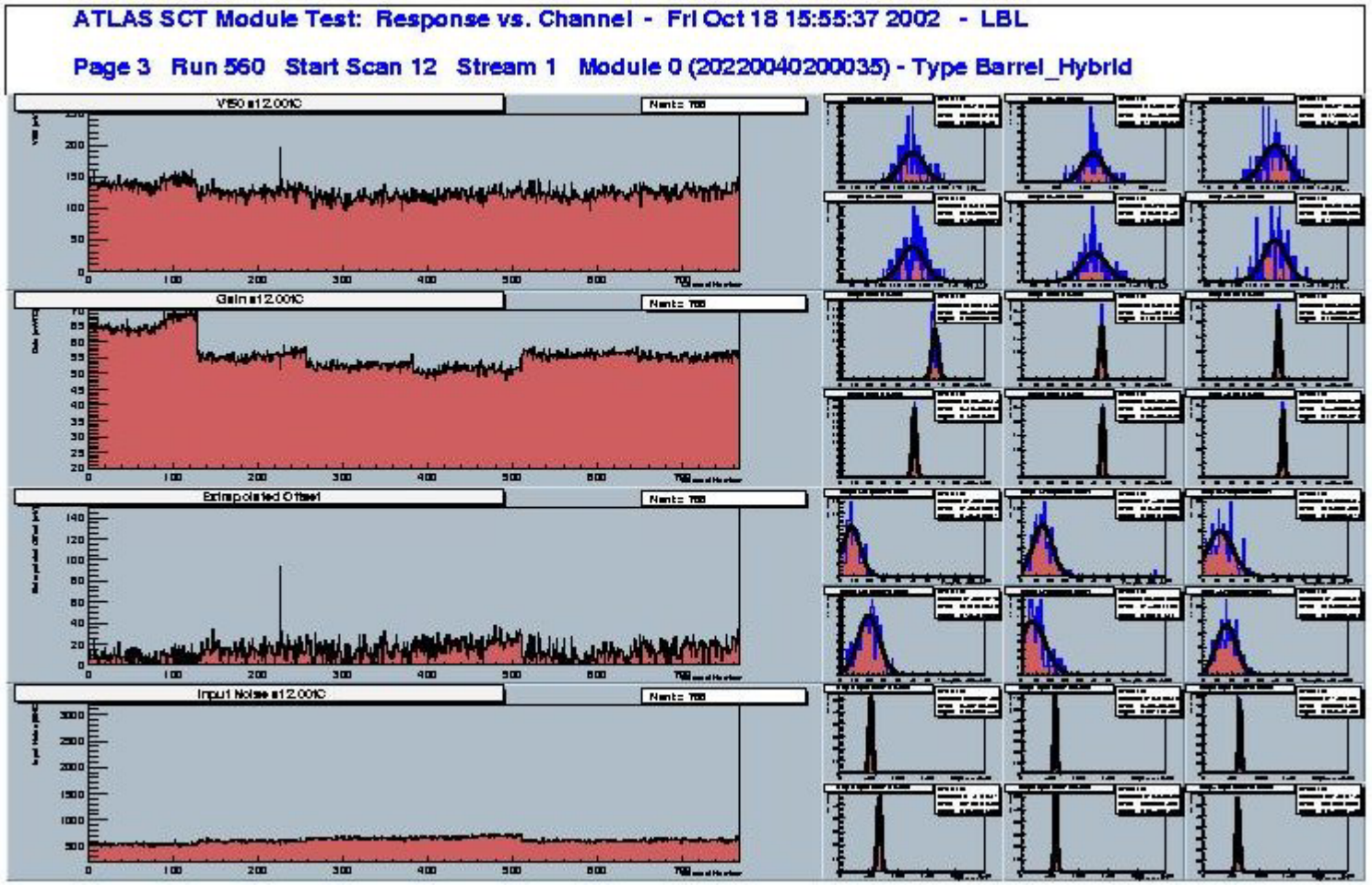
Hybrid 20220040200022
Chip 10 High Offset



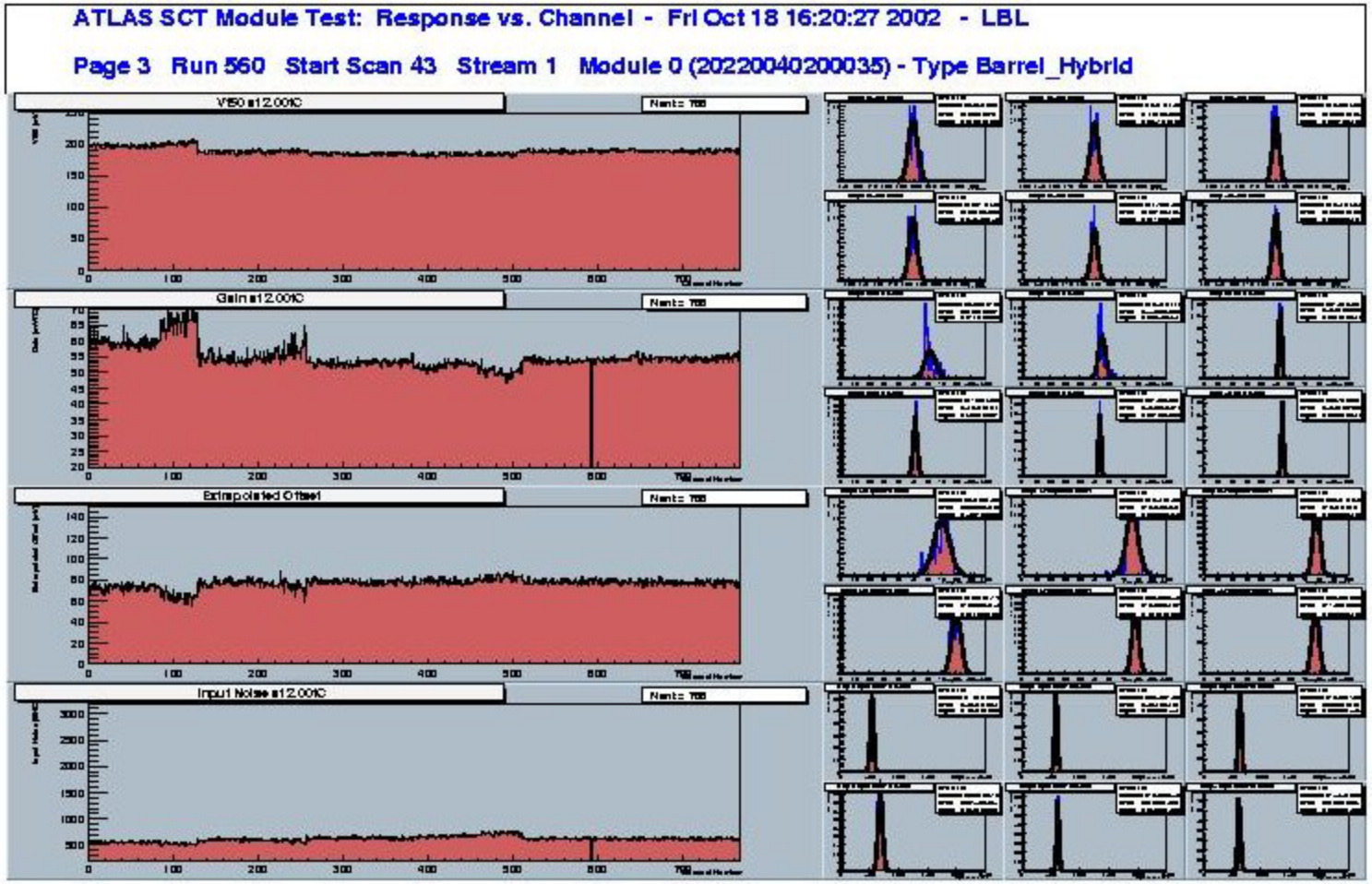
Hybrid 20220040200022
Wafer/Hybrid Comparison



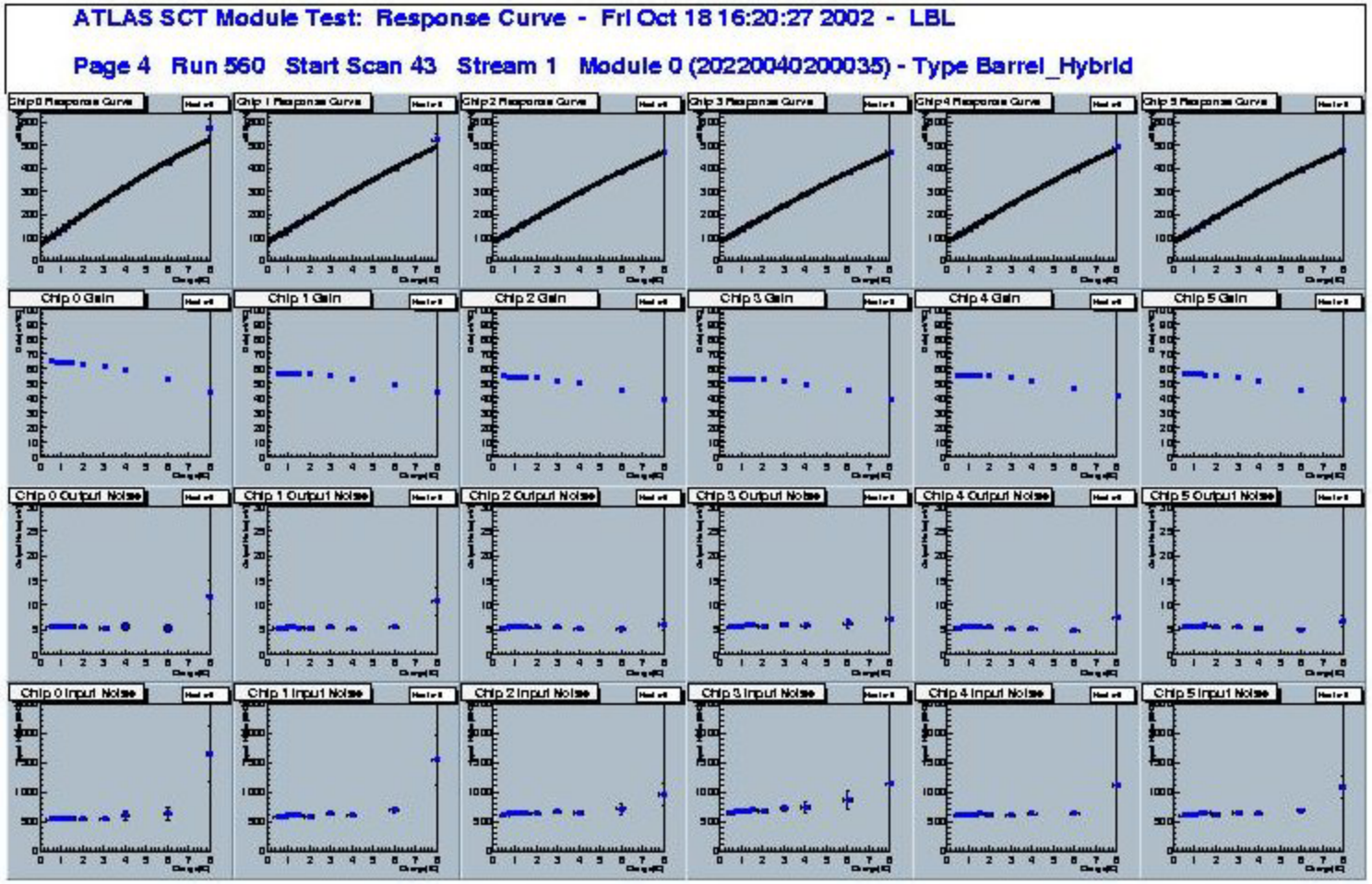
Hybrid 20220040200035
Chip 6 (M8) High Gain (3Pt)



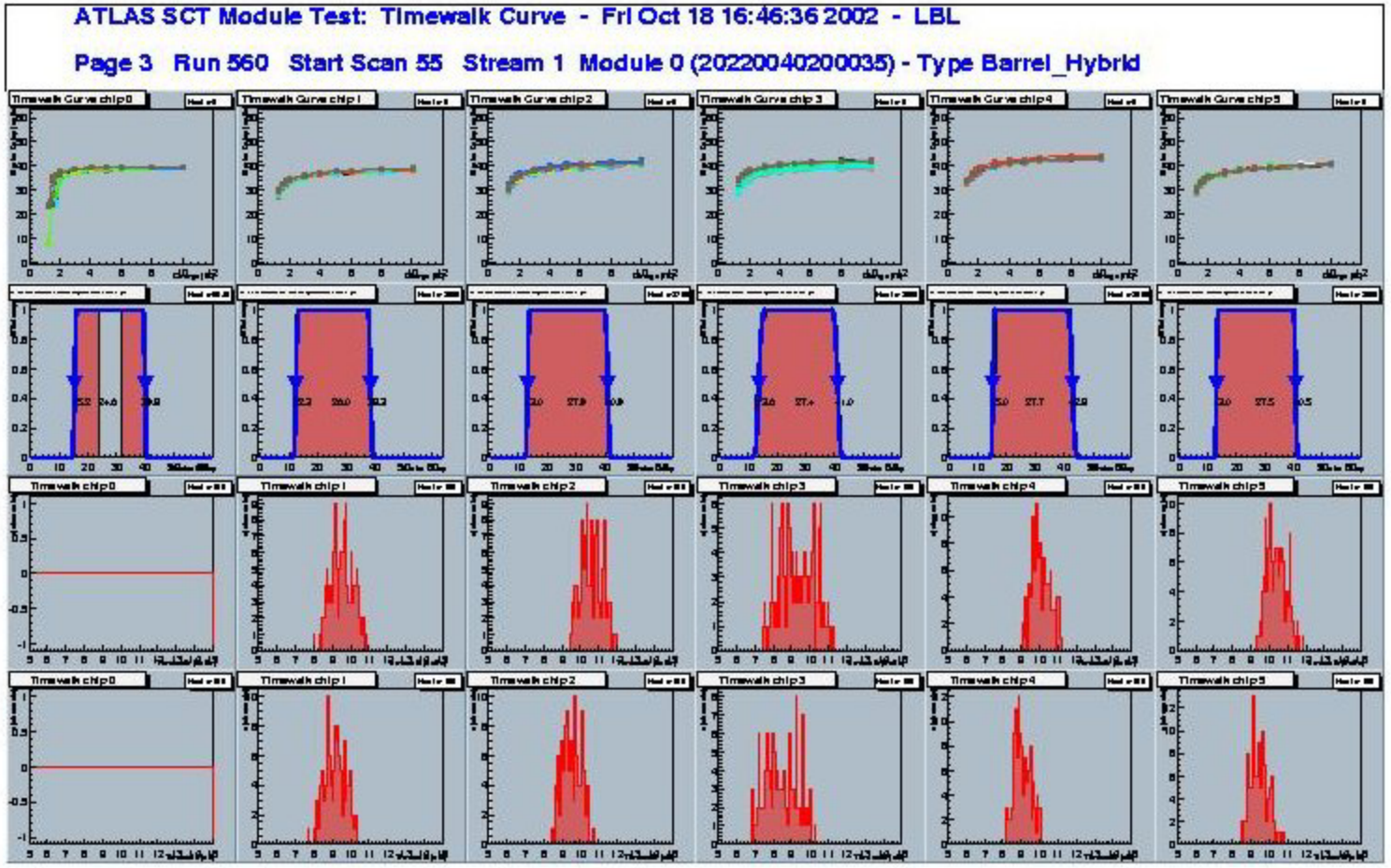
Hybrid 20220040200035
Chip 6 (M8) High Gain (After trim)



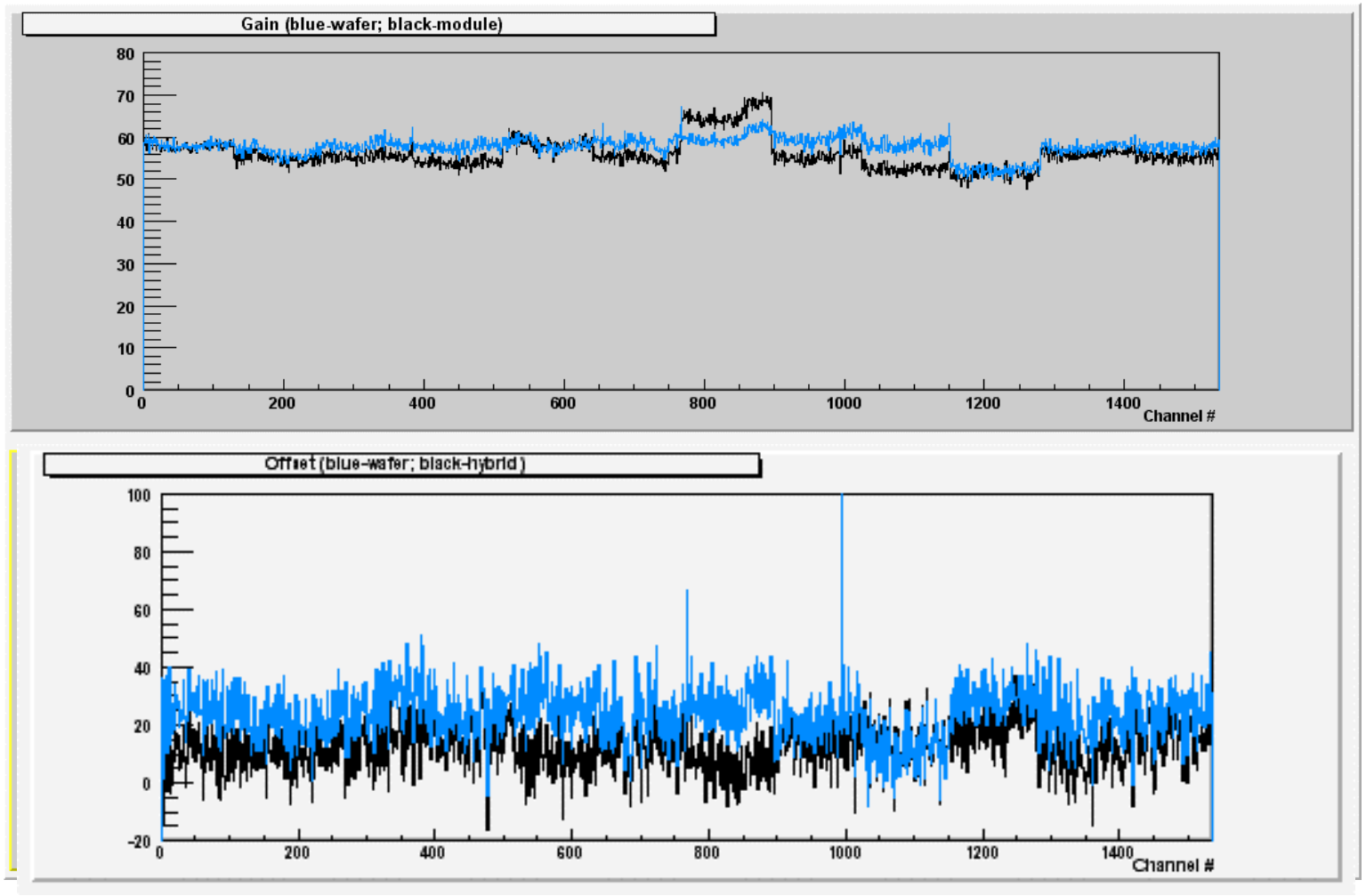
Hybrid 20220040200035
Chip 6 (M8) High Gain (after trim)



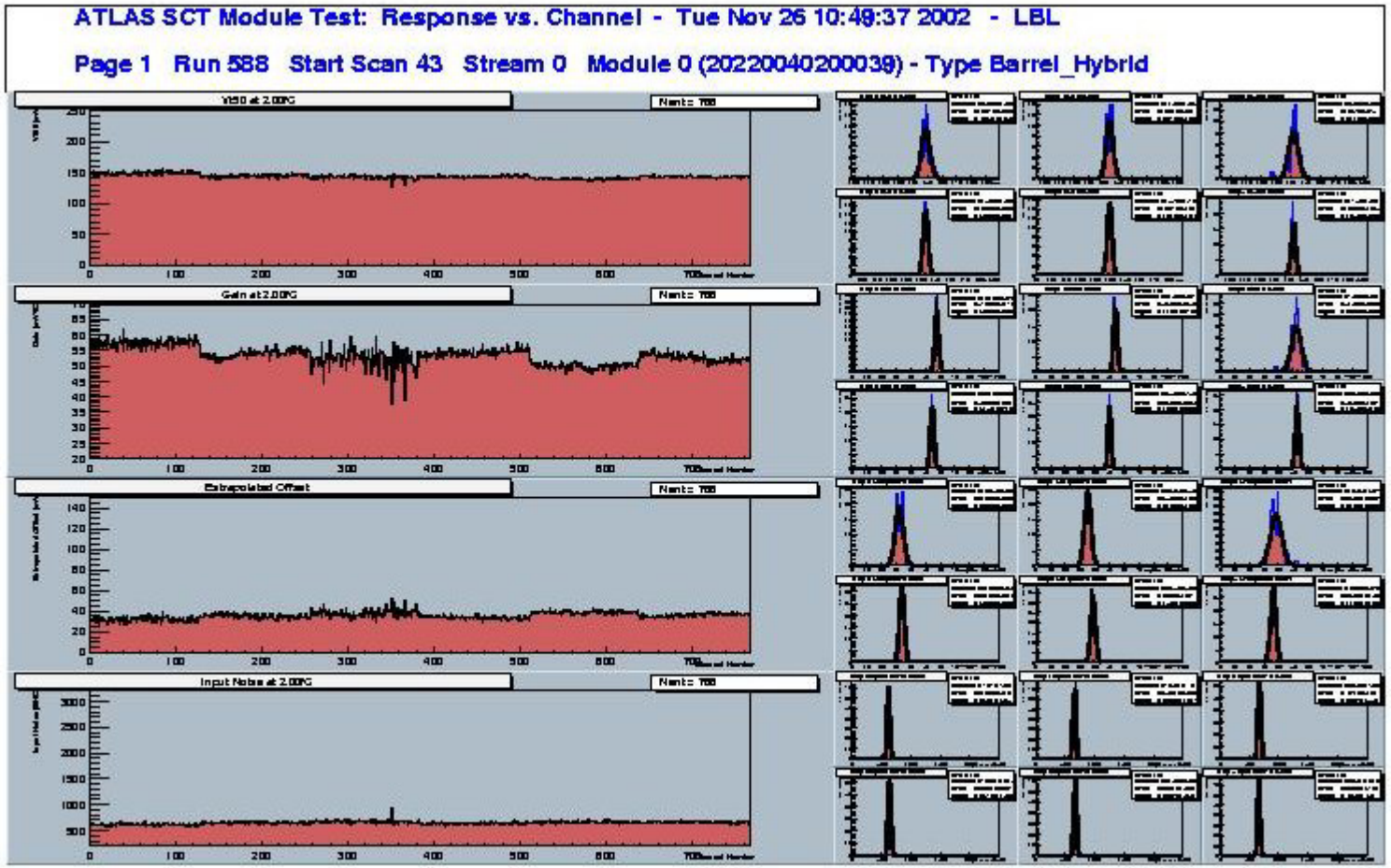
Hybrid 20220040200035
Chip 6 (M8) Time Walk Failure



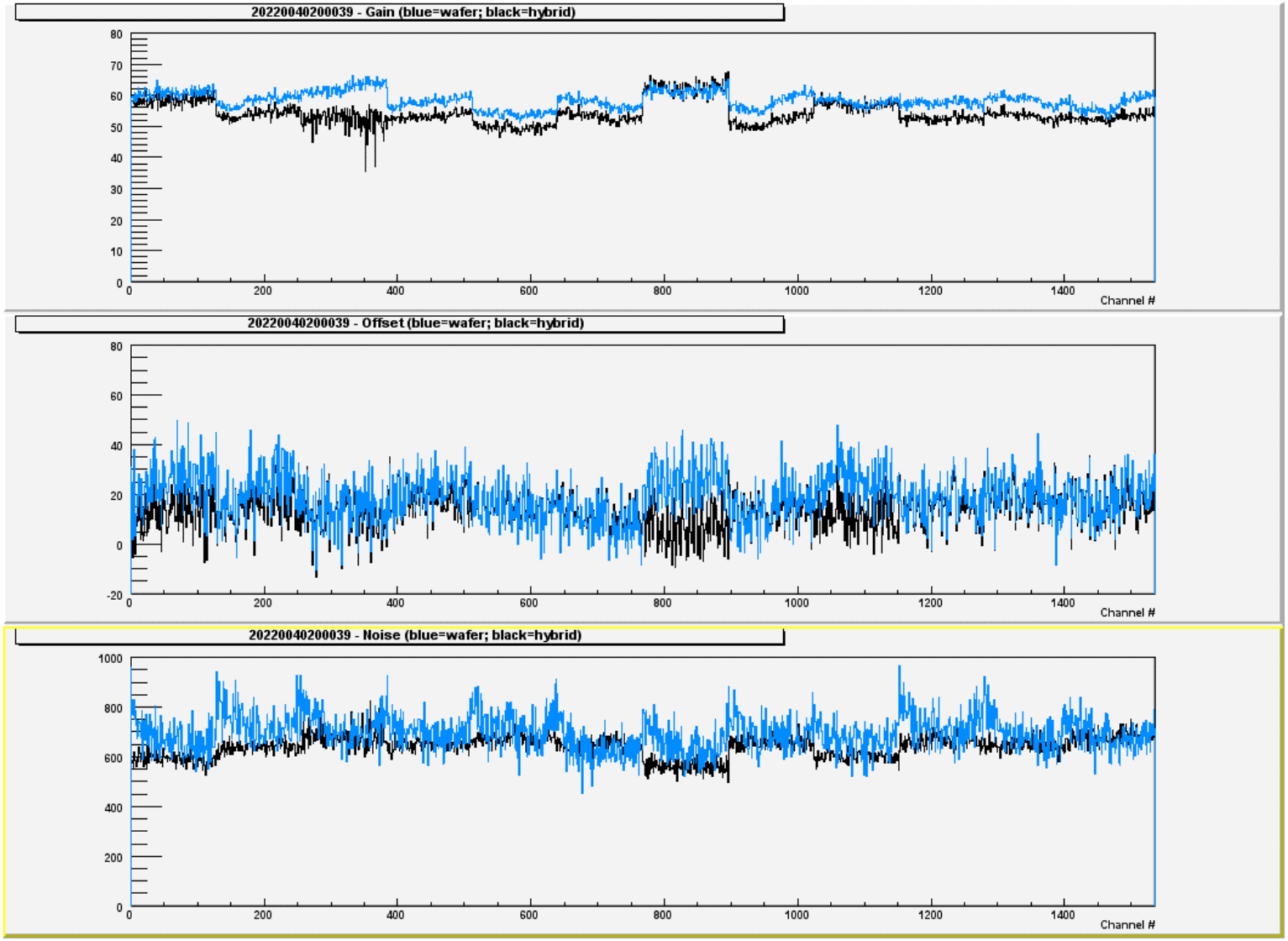
Hybrid 20220040200035
Wafer/Hybrid Comparison



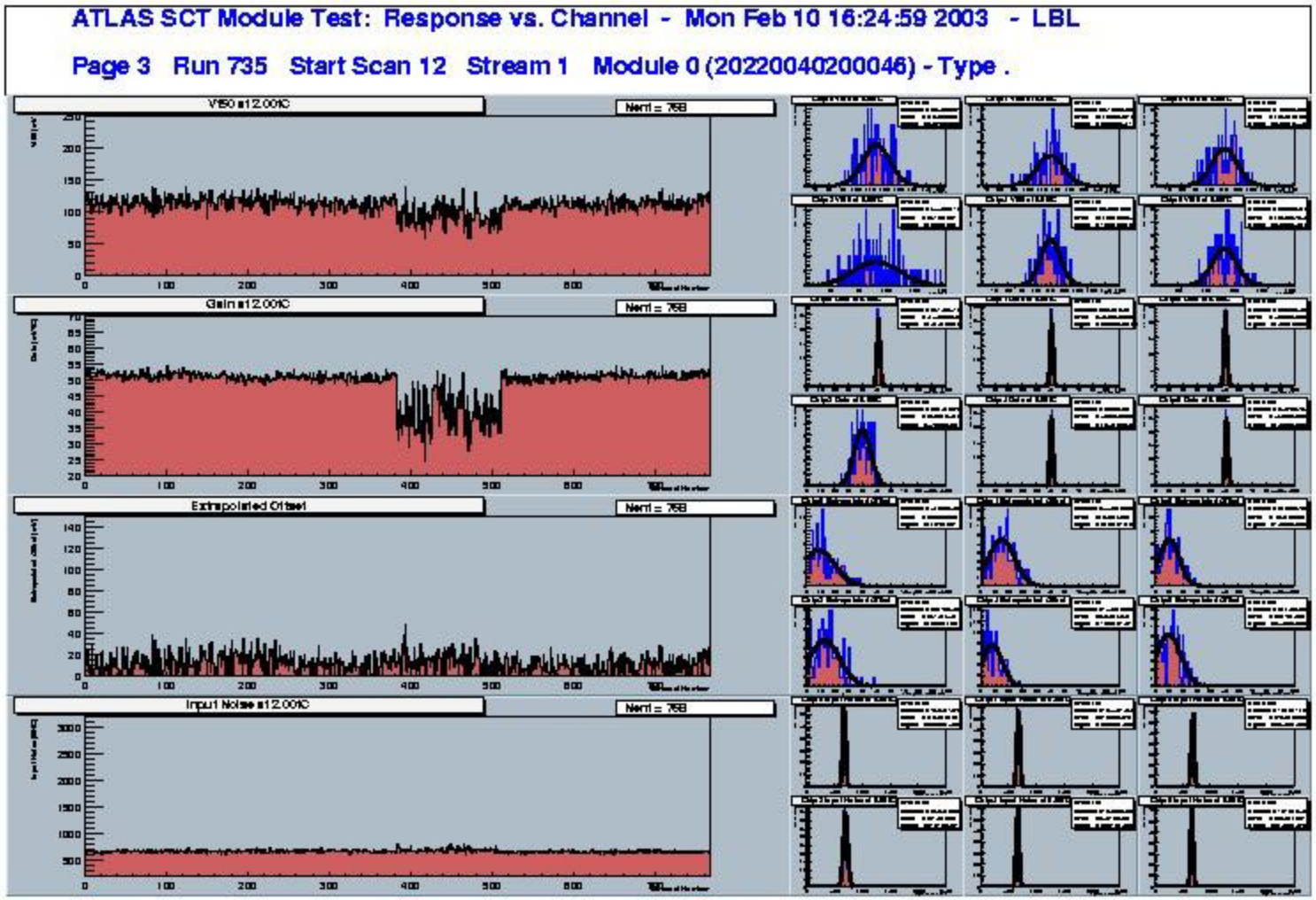
Hybrid 20220040200039
Chip 1 Large Gain Spread



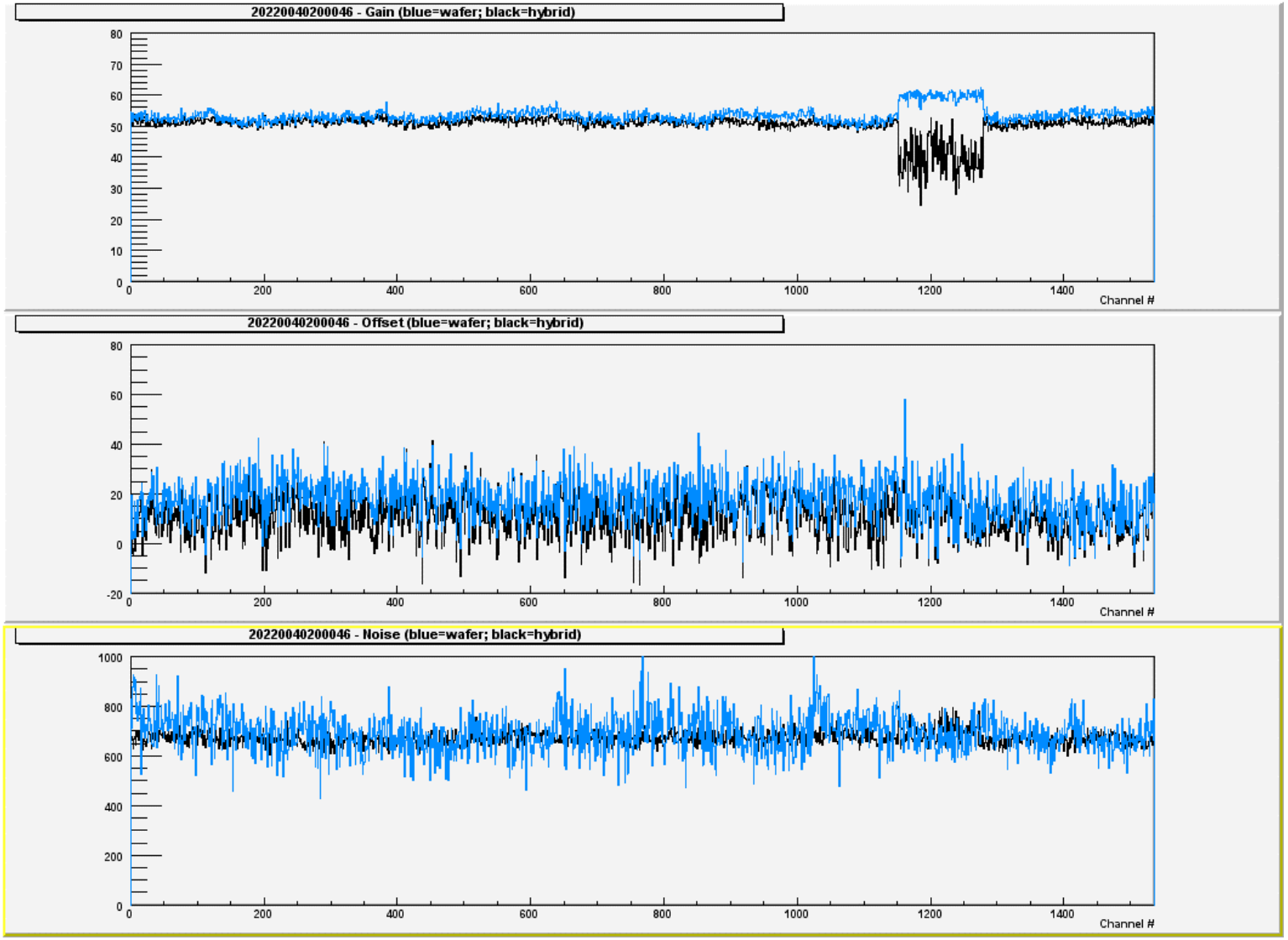
Hybrid 20220040200039
Wafer/Hybrid Comparison



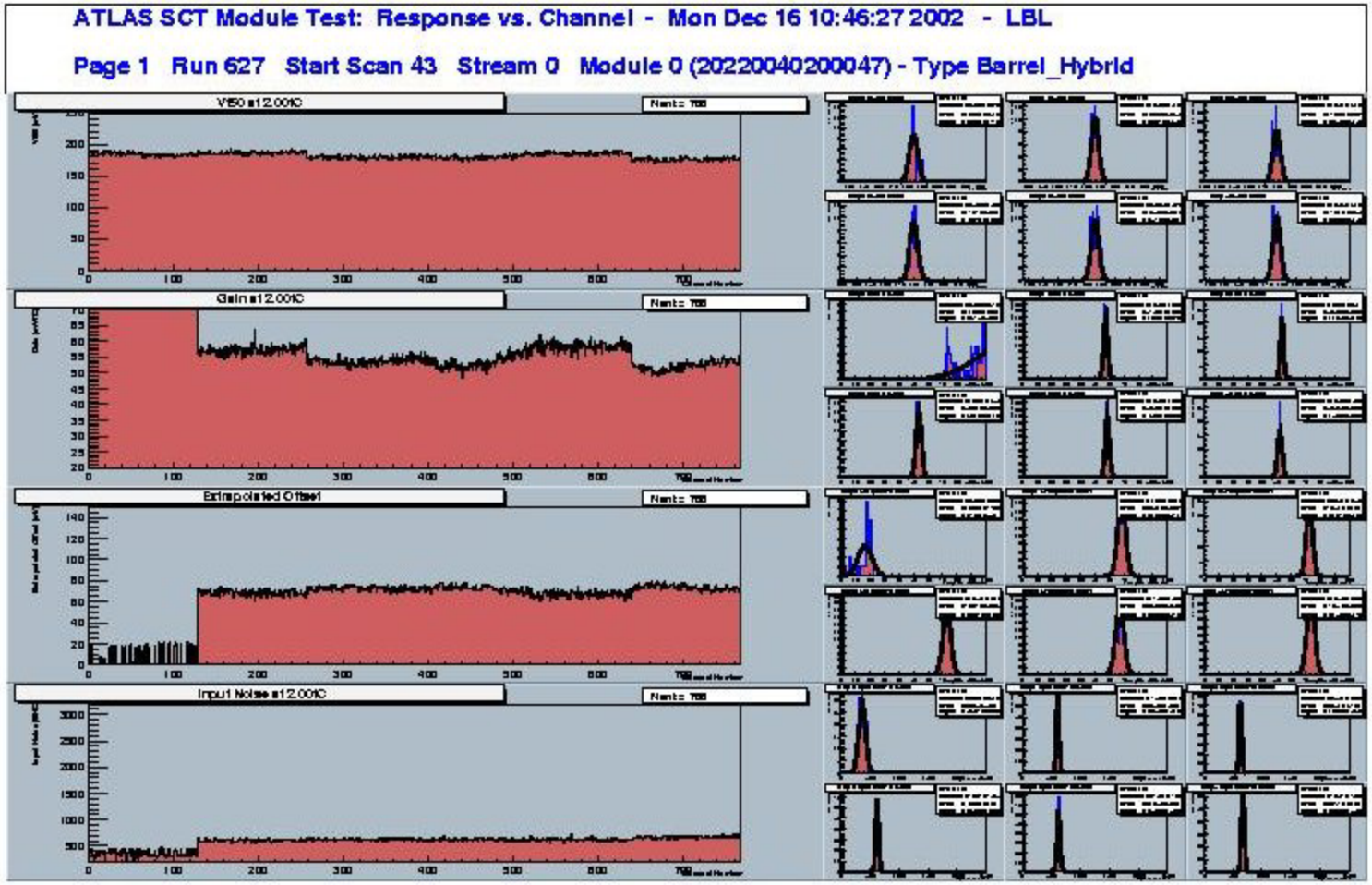
Hybrid 20220040200046
Chip 9 Large Gain Spread



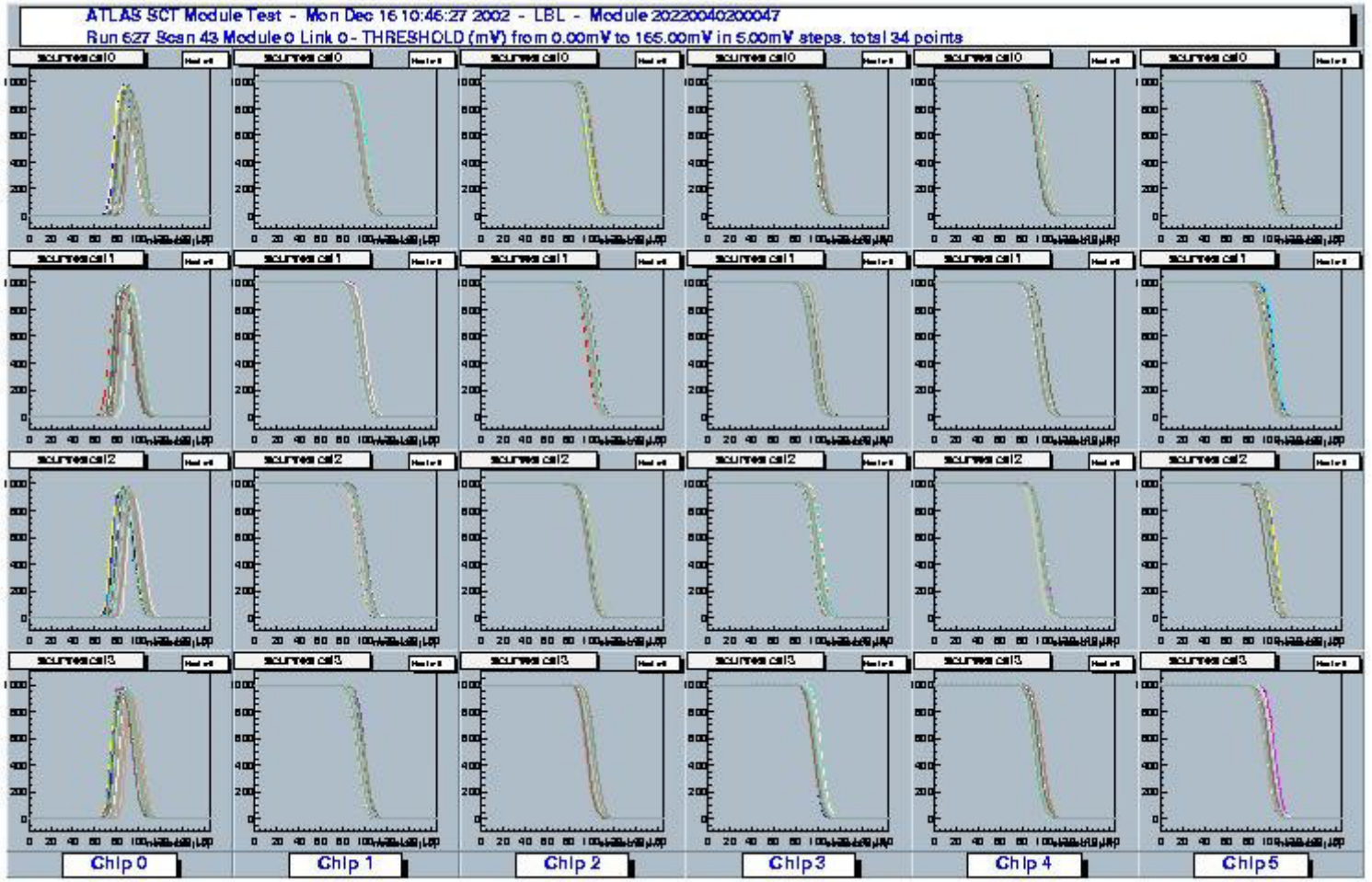
Hybrid 20220040200046
Wafer/Hybrid Comparison



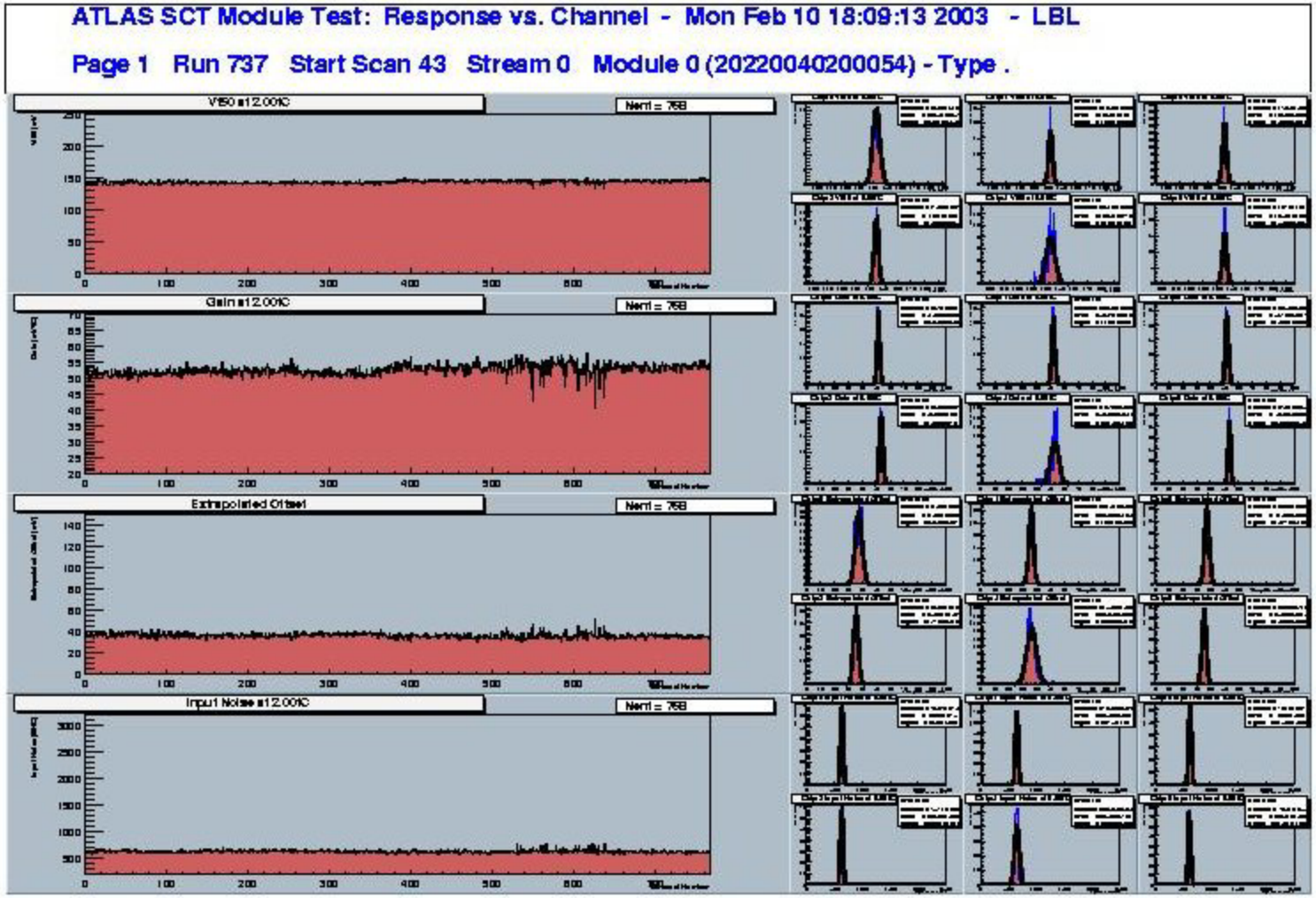
Hybrid 20220040200047
Chip 6 Trim DAC Loading



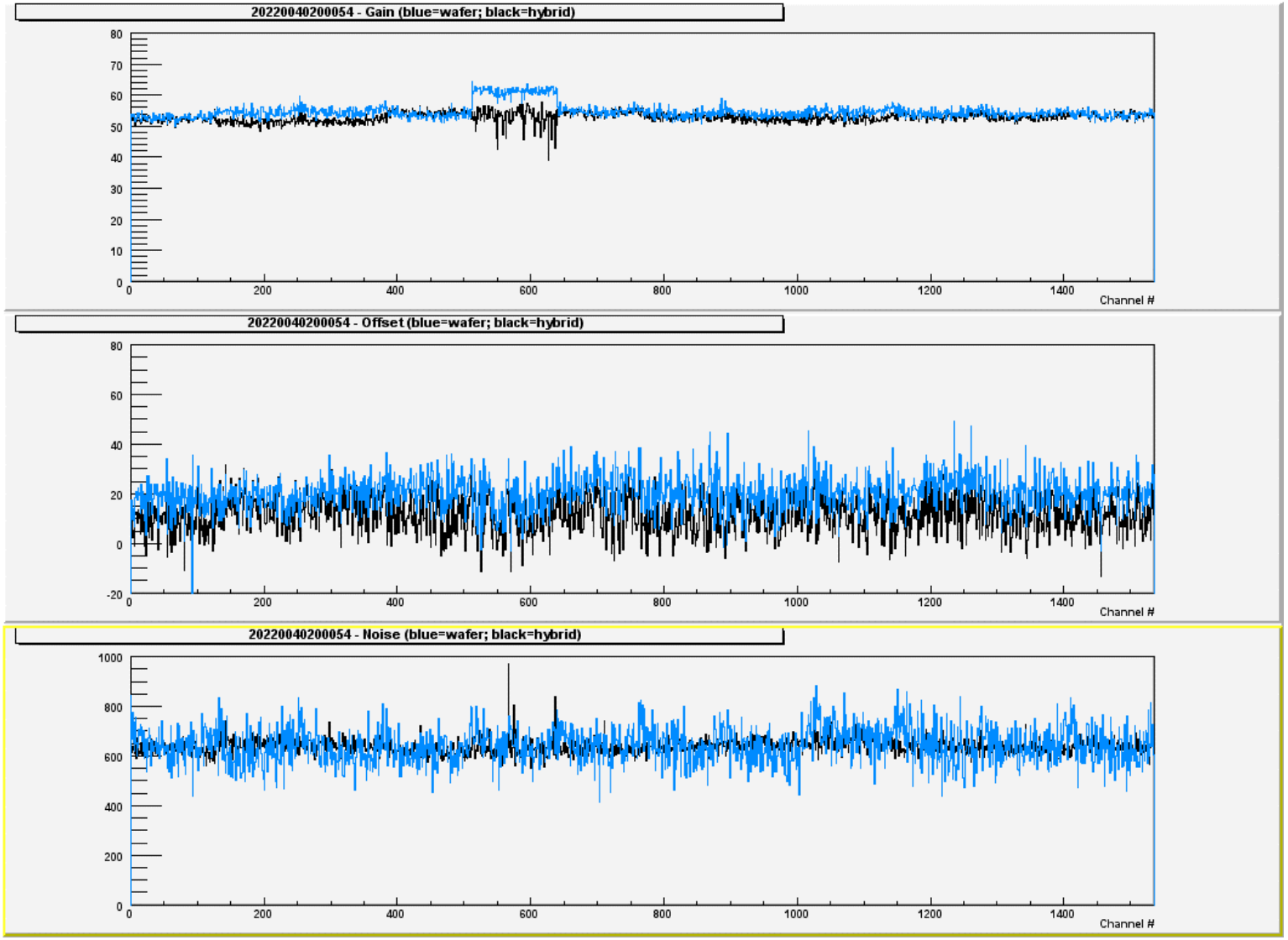
Hybrid 20220040200047
Chip 6 Trim DAC Loading



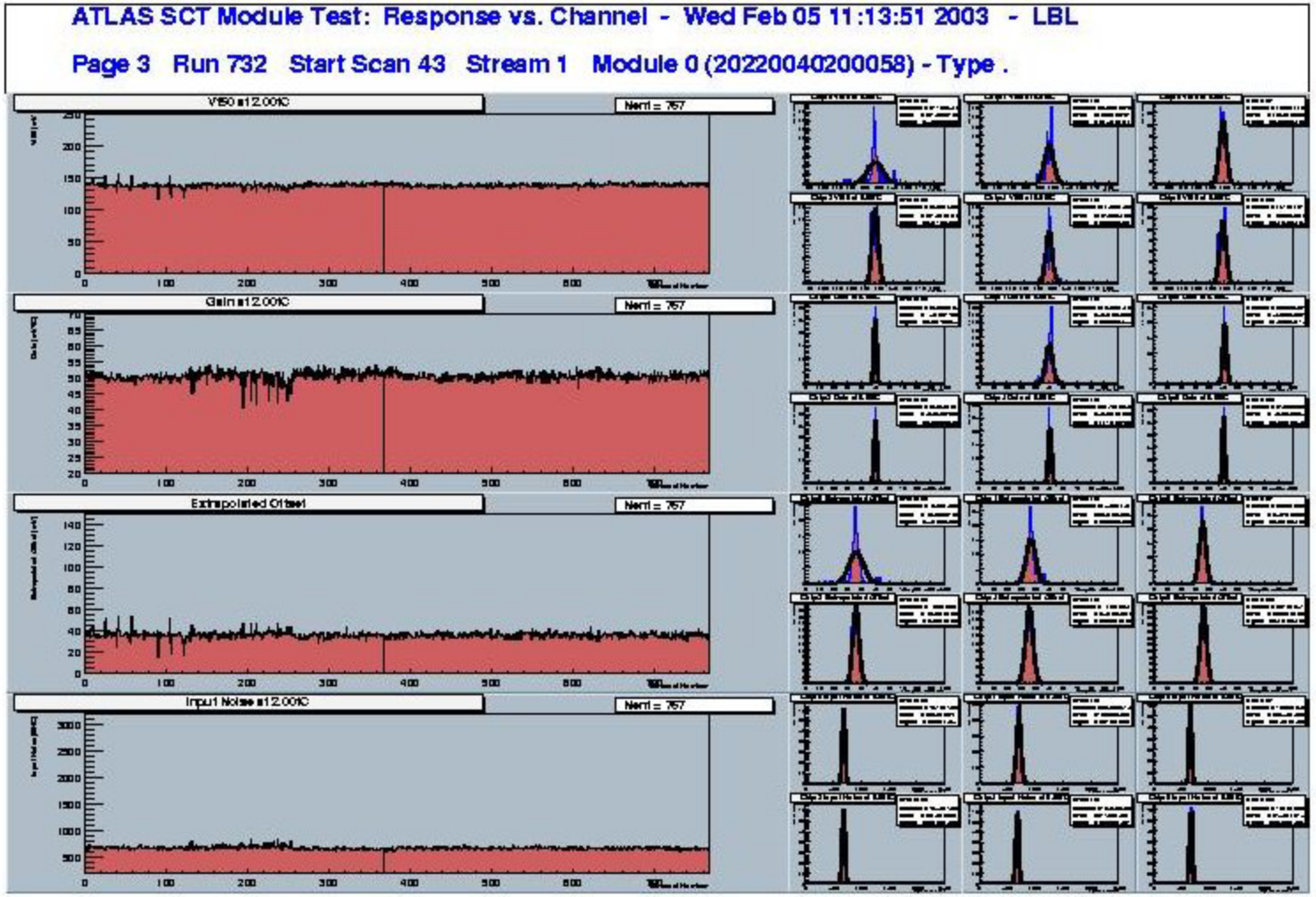
Hybrid 20220040200054
Chip 6 Large Gain Spread



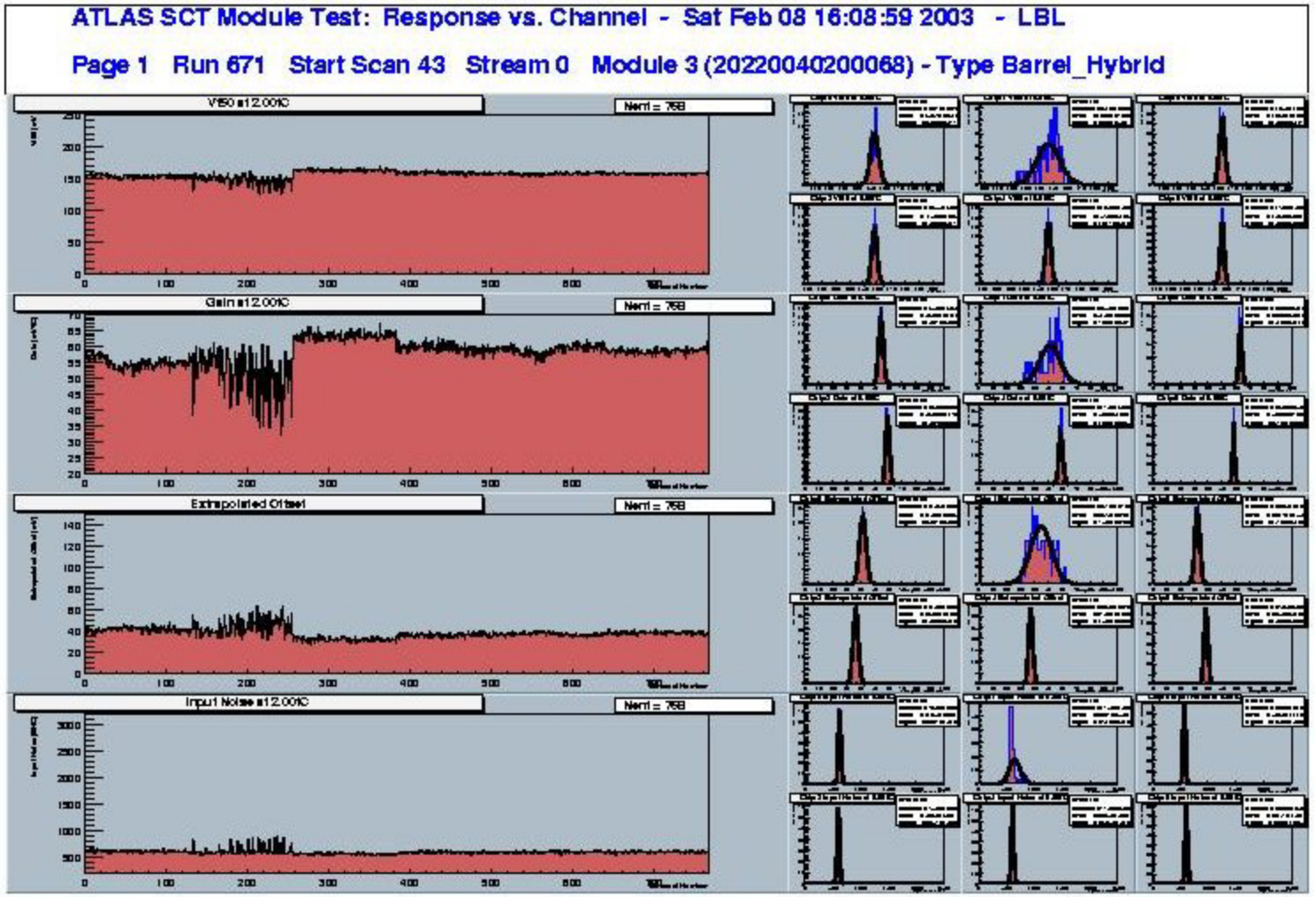
Hybrid 20220040200054
Wafer/Hybrid Comparison



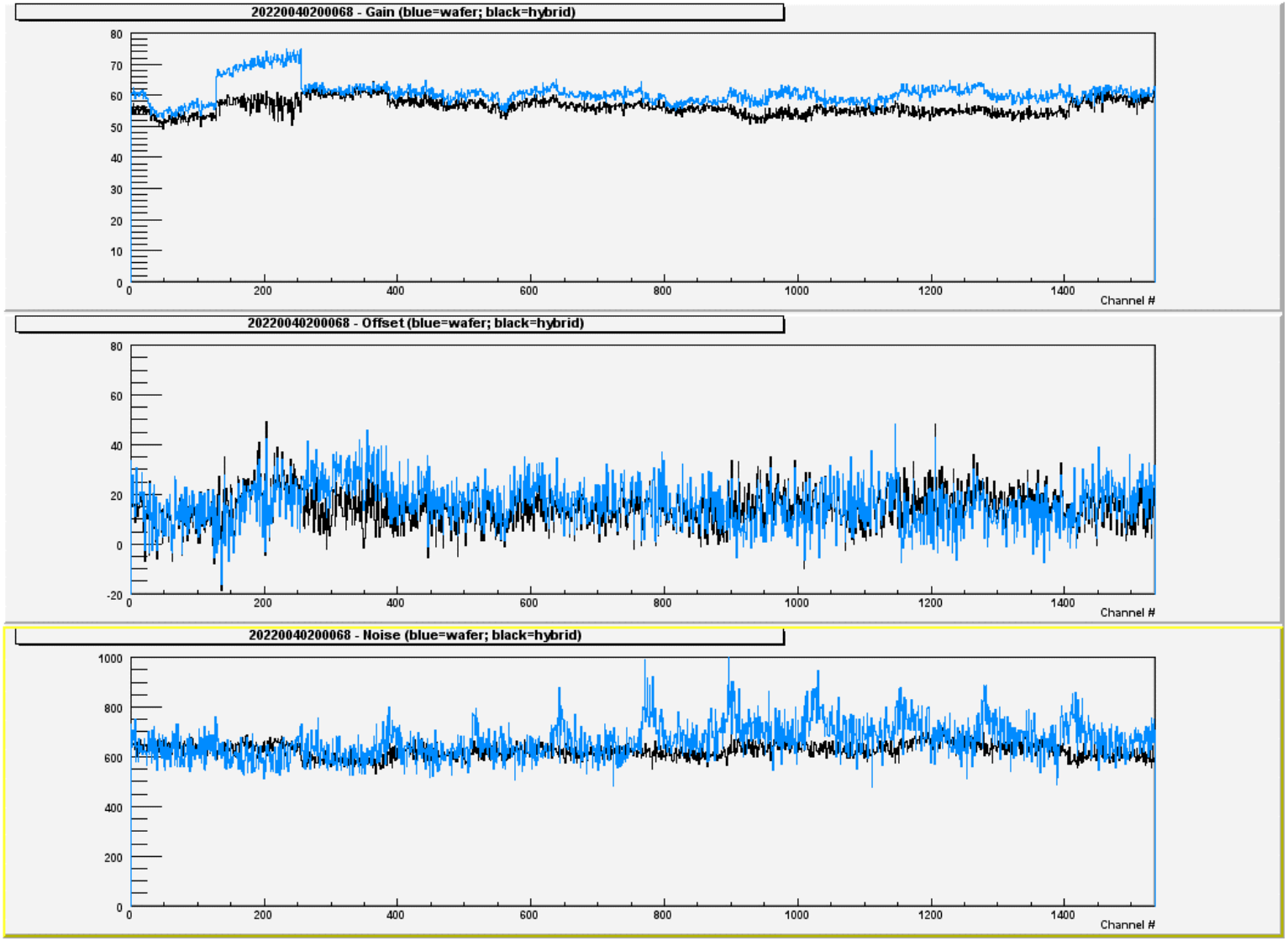
Hybrid 20220040200058
Trim DAC Loading



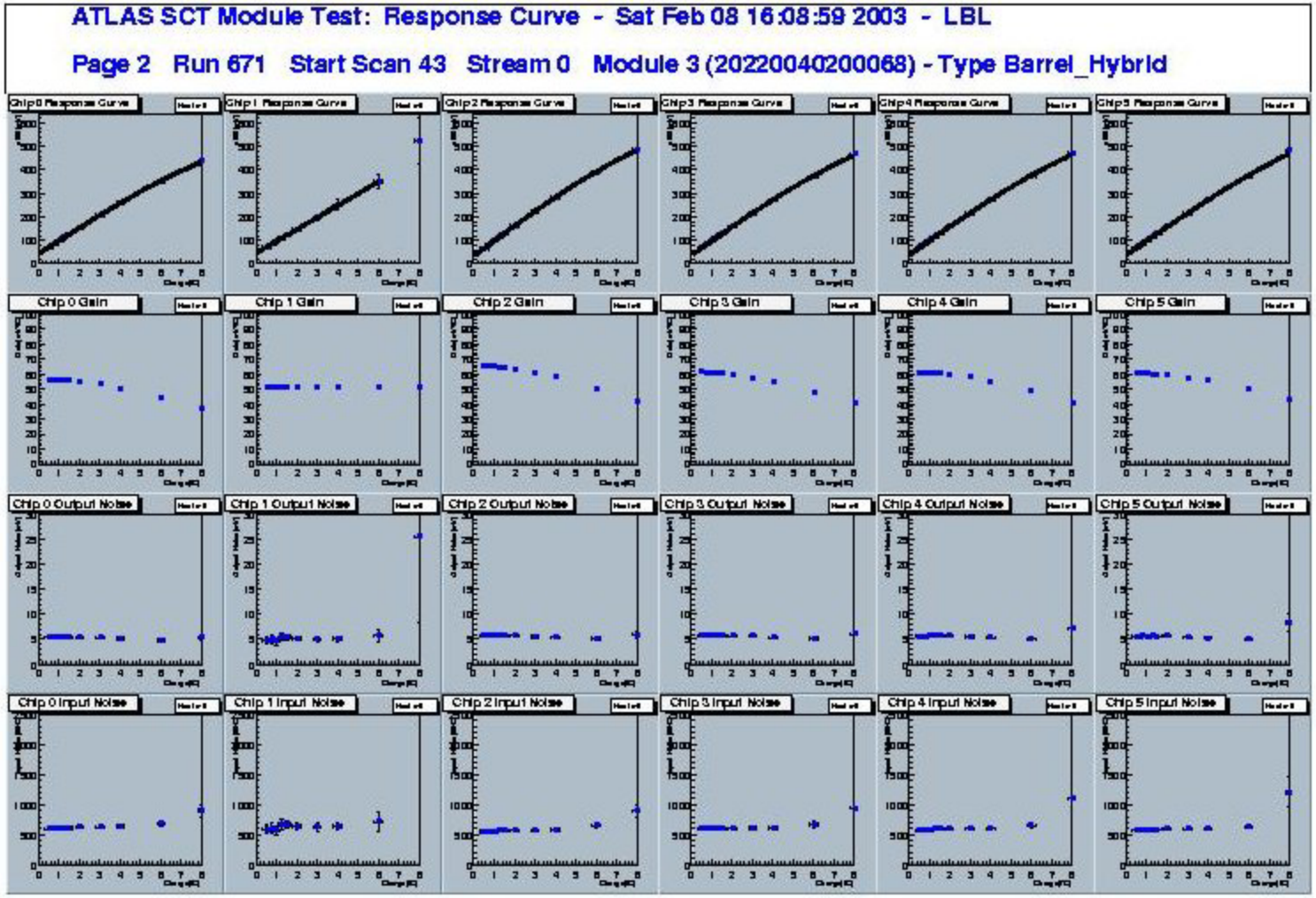
Hybrid 20220040200068
Chip 6 Large Gain Spread - cold



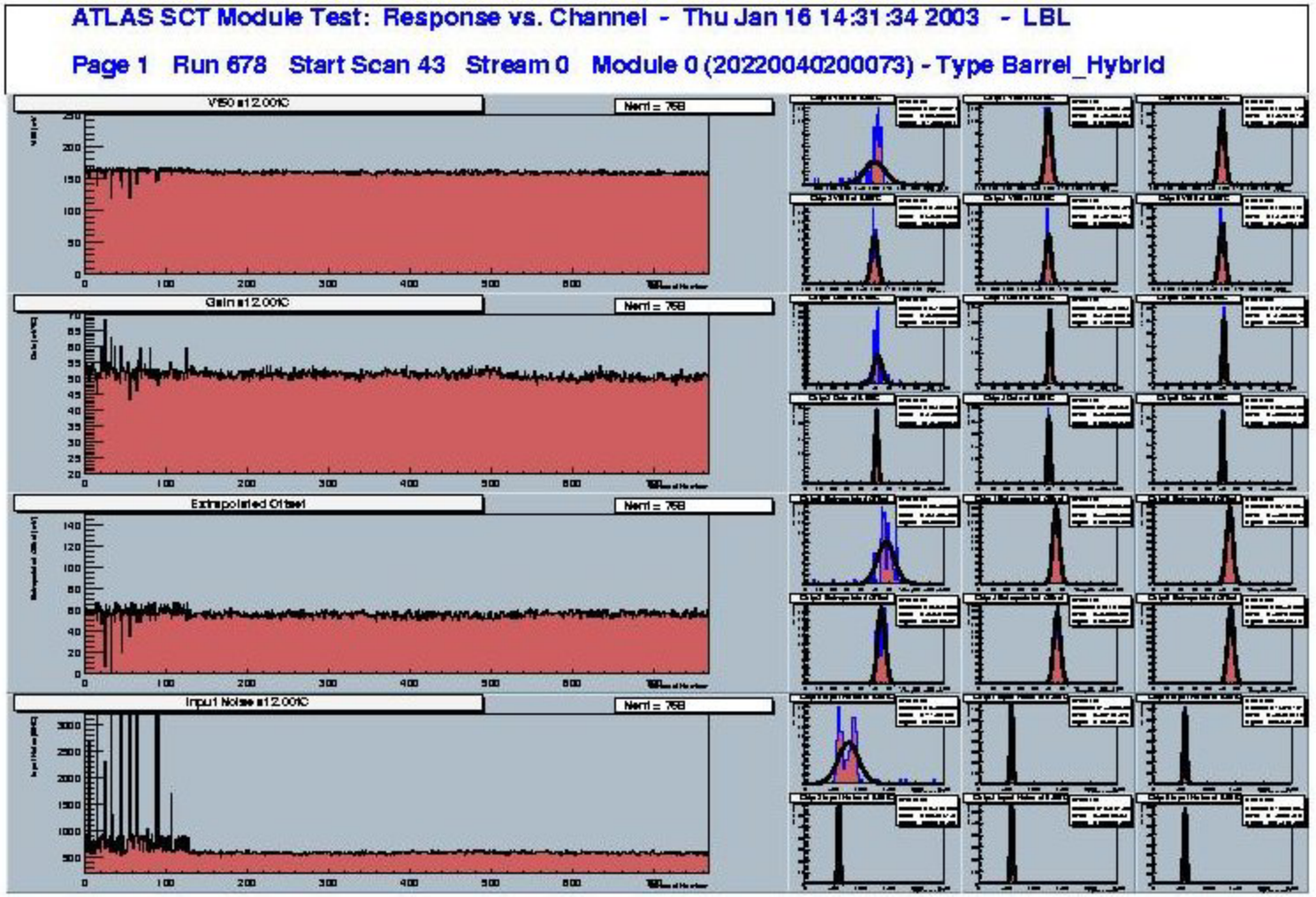
Hybrid 20220040200068
Wafer/Hybrid Comparison



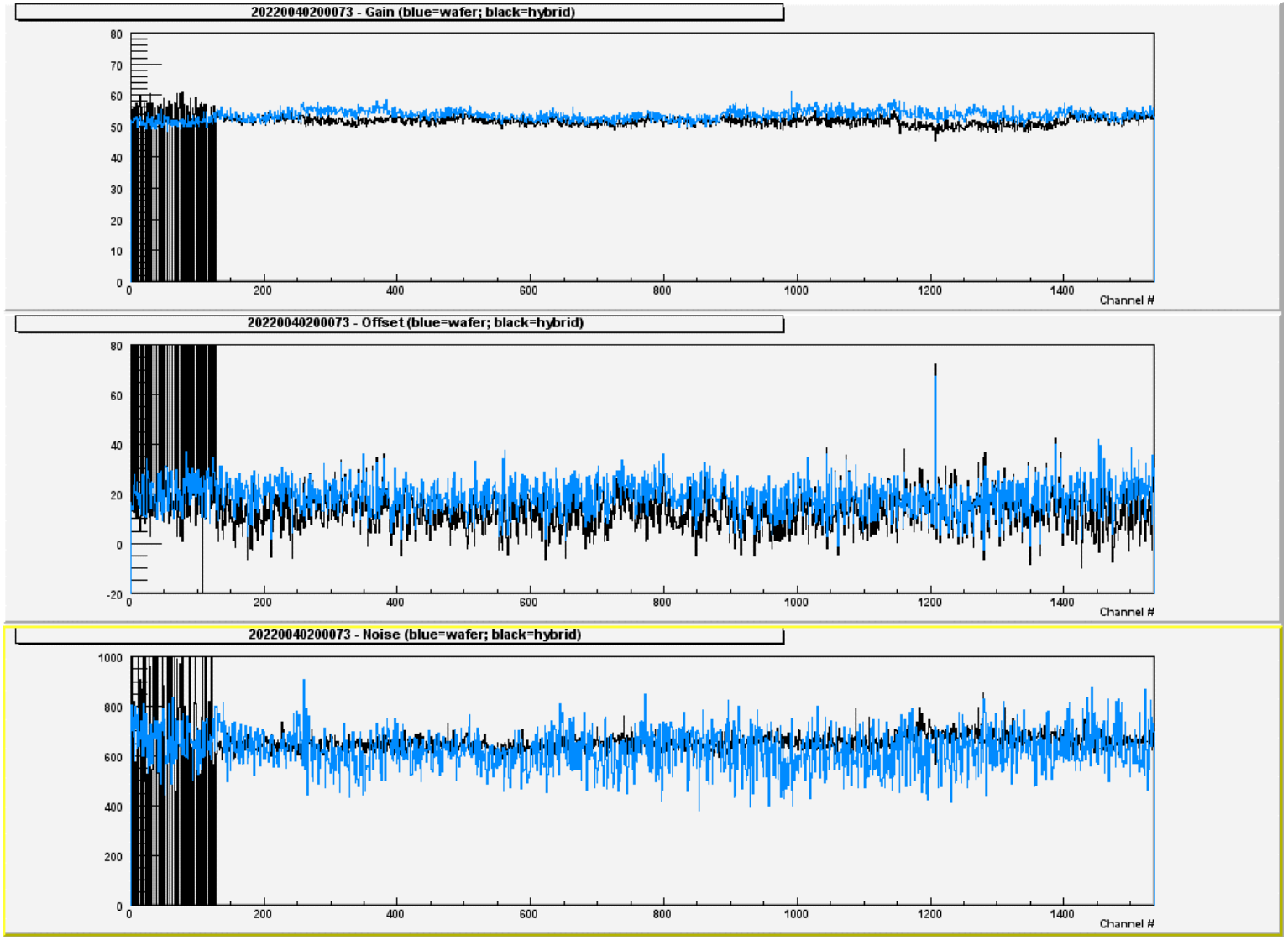
Hybrid 20220040200068
Chip 6 Large Gain Spread - cold



Hybrid 20220040200073
Chip 0 Strobe delay

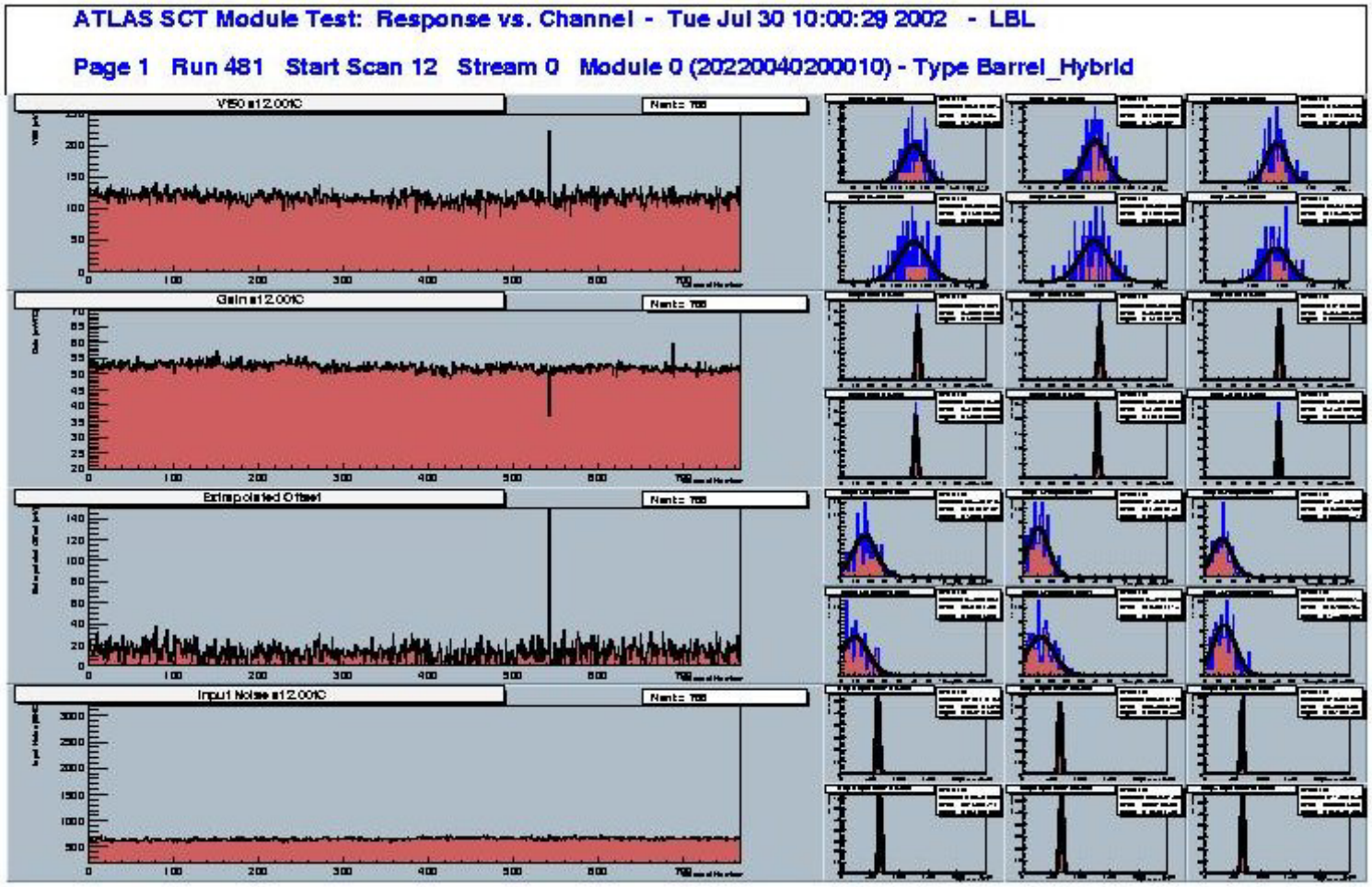


Hybrid 20220040200073
Wafer/Hybrid Comparison



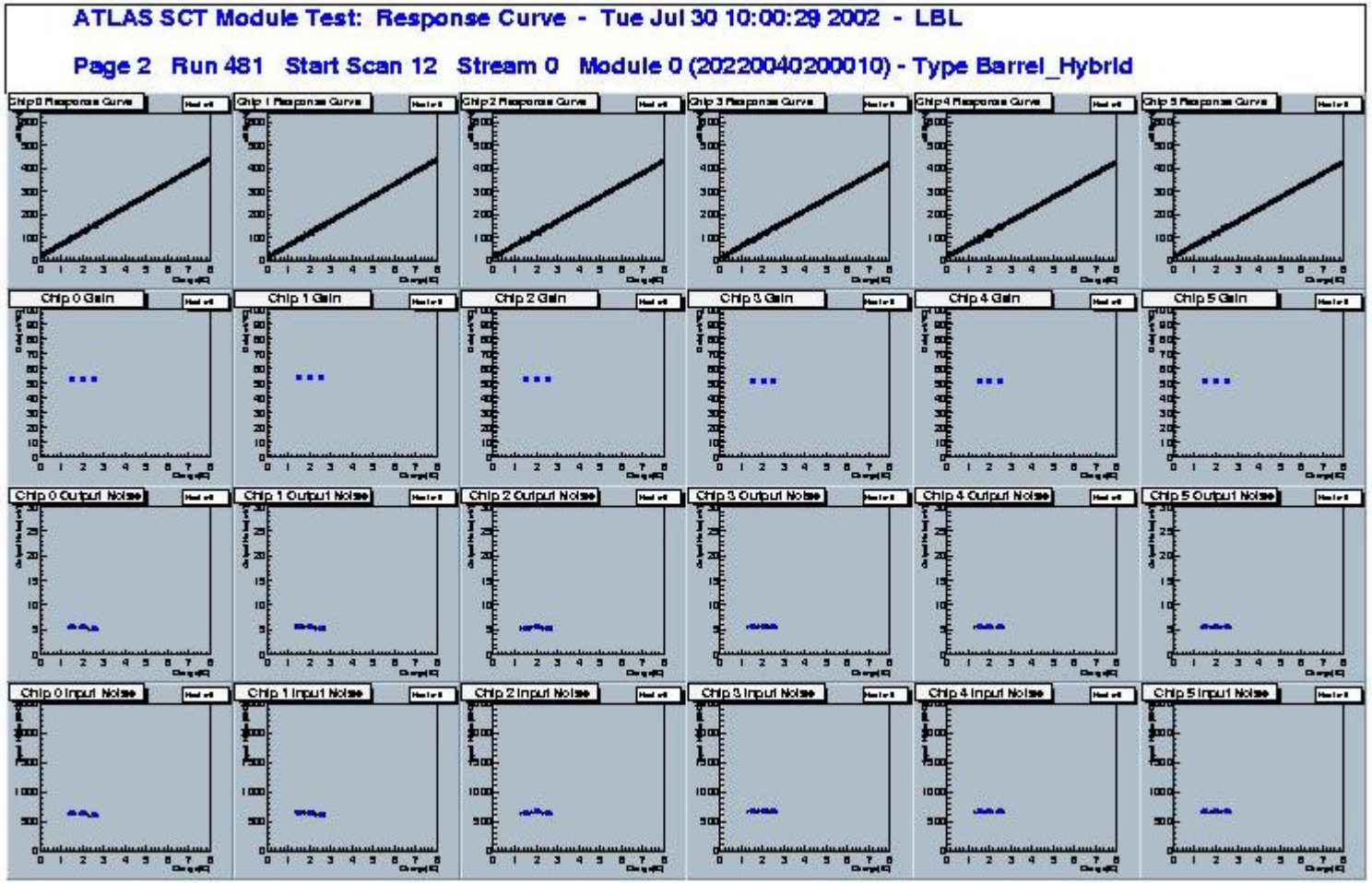
Hybrid 20220040200010

High Offset (low gain)



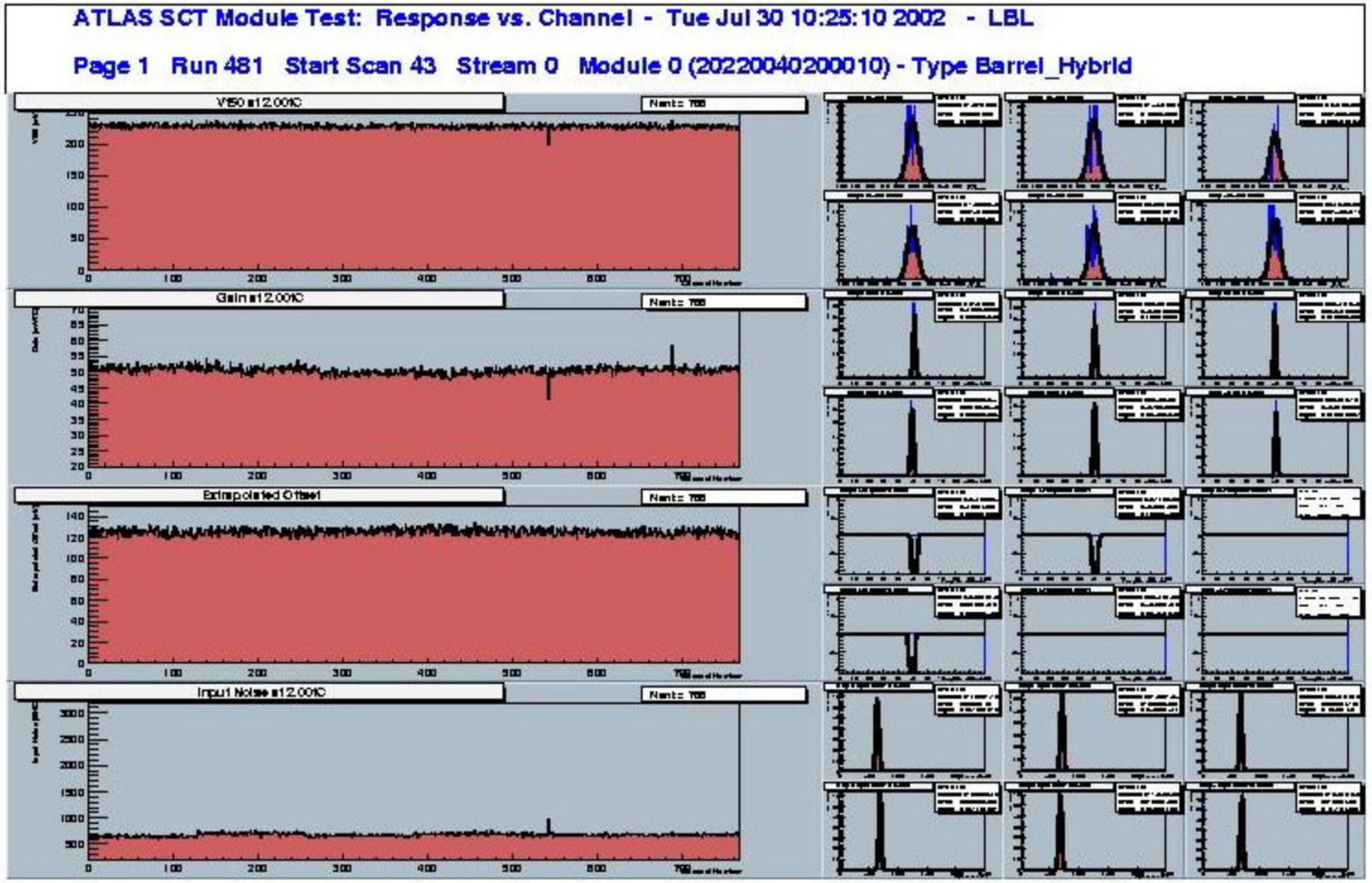
Hybrid 20220040200010

High Offset (low gain)



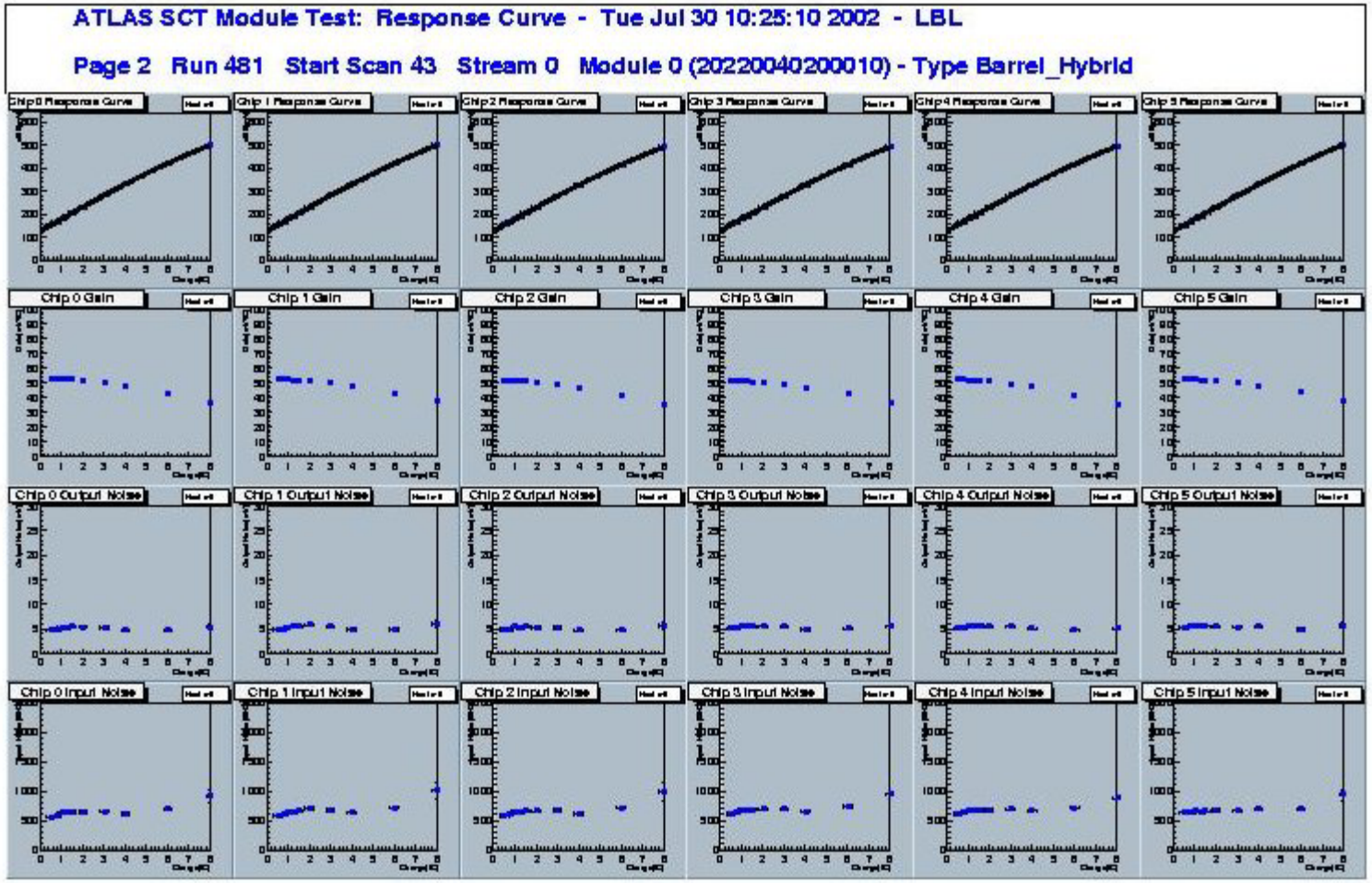
Hybrid 20220040200010

High Offset (low gain)

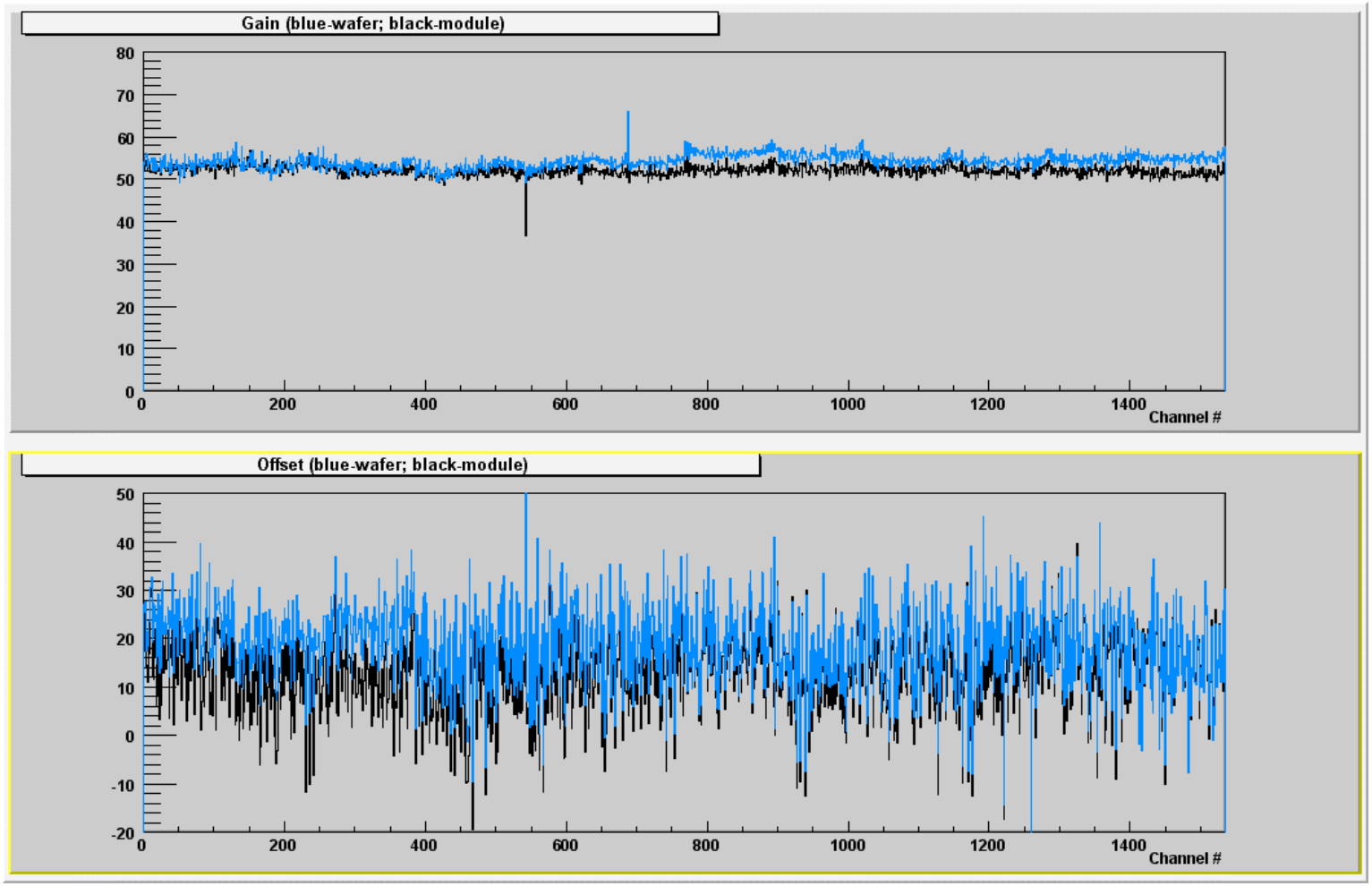


Hybrid 20220040200010

High Offset (low gain)



Wafer/Hybrid Comparison
Hybrid 20220040200010



Chip Response – New Cuts

- New cuts in the TrimRange Scan algorithm

- Noisy channels are now identified by the cut 1.15*(chip mean noise)

- Code to automatically exclude suspect data due to "8fC effect"
  The fitted range is adjusted to exclude points (charge > 5.0fC)
  for which the output noise is > 1.5*the mean output noise taken over all charges

- Channels with anomalous gain are now identified as follows:
  hi_gain channels have gain greater than (1.25 * mean_chip_gain)
  lo_gain channels have gain less than (0.75 * mean_chip_gain).
  This is in agreement with the gain cuts used during chip testing.

Overall Issues

- **Gain non-uniformity** (but mostly in agreement with wafer data)
  - Wafer/Hybrid Comparison to confirm chips are within spec
  - Possible chip pre-selection/better matching from looking at Wafer data of chips available to use

- **Large Gain spread** for several chips on a given hybrid at 0°C (Hybrid LTT) after trim
  - The threshold DAC has a tendency to saturate.
  - This effect kicks in at slightly lower thresholds as a hybrid is cooled down.
  - The 8fC point is out of line (off to higher threshold) during low temperature tests.
  - For some hybrids it can be seen also at room temperature.
  - This can effect the fitting of the response curve, hence the false high gain.
  - Not including the 8fC point in the RC fit helps.
  - Only 1 chip lost at cold (20220040200068)

- **LTT time**
  - LTT- Burn-in test results show no time dependence for defects
    - Any additional defects occur immediately:
    - 1 defective chips (large gain spread at cold)
    - 1 slow chip (at warm)
    - very few noisy/dead channels (almost none)

Summary

HYBRIDS

- **Defective Chips**

  12 chips defective after electrical testing + **2** damaged (chipped)

  Gain(6) Token(1) TW (1) Strobe Delay (1) TrimDAC (2) High Offset (1)
- **Wafer/Hybrid comparison**

  - used regularly and especially when anomalies are present
  - effective tool for chip selection
- New features/cuts in the software helps with anomalous chip response
- **LT-Tests** show no time dependence for defects: time could well be reduced to a few hours

MODULES

- **19 modules built** as of Feb 27 **+ 2** just assembled
- 17 modules completed with testing + 2 in progress
- **PA defect** on first batch of 29 hybrids
  - 15 hybrids already used in modules (11 rebonded)
  - 9 modules with 8-14 final unbonded channels (50% channel regained)
  - 14 hybrid still to be used but fixing bonds during rebonding -> good yield
  - 4 new hybrids used in modules
- HV boards communication/protocol more stable after Peter's upgrade of the software
- **No additional defect found in modules through sequence of tests**