# **ASIC Production Status**

SCT Week 10-Oct-2001

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#### **Production of ABCD has Started**

Production Readiness Review was passed on 4-Jul-01.

Generally, we received good marks for being prepared for production.

Concern was raised about outstanding radiation issues, especially the increases in  $I_{\rm dd}.$  Further studies were strongly recommended.

**Recommendations:** 

Add total ionization dose (TID) test to the QA plan in addition to the NIEL (neutron) test already in the plan.

An X-ray test program is being developed at CERN to fulfill this recommendation.

A more complete plan for SEU mitigation in the experiment should be formulated and the SEU rate for both polarities of upset should be verified.

An accelerated life test on a limited number of modules or chips should be made.

Meeting was held with ATMEL to finalize contract issues and delivery schedules on 5-Jul-01.

Authorization to start fabrication of first 520 wafers has been given.

The first 35 production wafers were received at CERN on 28-Aug.

#### **Production Plan Actuals**

Wafers are received at CERN and then sent to the test sites.

**Cumulative Actuals Report for wafer orders and wafer deliveries:** 

Week	Week of	<b>Raw Wafers</b>	Fabrication	Wafers Received
Number		Released	Released	by CERN
40	30-Sep-00	520		
		520		
28	09-Jul-01	520	520	
29	16-Jul-01	675	520	
30	23-Jul-01	675	520	
31	30-Jul-01	675	520	
32	06-Aug-01	675	520	
33	13-Aug-01	675	520	
34	20-Aug-01	675	520	0
35	27-Aug-01	675	520	35
36	03-Sep-01	675	520	35
37	10-Sep-01	675	520	35
38	17-Sep-01	675	520	35
39	24-Sep-01	675	520	35

CERN's wafer screening facility is temporarily not available. 31 of the first 35 wafers were sent to RAL and UCSC for testing. The remaining 4 were left at CERN for X-ray testing.

## **Production Plan Actuals**

**Cumulative Actuals Report for wafer test activity at RAL:** 

Week	Week of		A	t RAL				
Number		Wfrs@RAL	WfrsTested	WfrsCut	GoodDice	DiceShpd	<b>DiceTo: Forward</b>	UK-B
28	09-Jul-01							
29	16-Jul-01							
30	23-Jul-01							
31	30-Jul-01							
32	06-Aug-01							
33	13-Aug-01							
34	20-Aug-01							
35	27-Aug-01							
36	03-Sep-01	15	2					
37	10-Sep-01	15	5	0	0	0	0	0
38	17-Sep-01	15	7	0	0	0	0	0
39	24-Sep-01	15	12	0	0	0	0	0

#### **Production Plan Actuals**

**Cumulative Actuals Report for wafer test activity at UCSC:** 

Week	Week of		A	t UCSC						
Number		Wfrs@UCSC	WfrsTested	WfrsCut	GoodDice	DiceShpd	DiceTo: LBNL	Japan	Scand.	Forward
28	09-Jul-01									
29	16-Jul-01									
30	23-Jul-01									
31	30-Jul-01									
32	06-Aug-01									
33	13-Aug-01									
34	20-Aug-01									
35	27-Aug-01	16								
36	03-Sep-01	16								
37	10-Sep-01	16	0	0	0	0	0	0	0	0
38	17-Sep-01	16	10	0	0	0	0	0	0	0
39	24-Sep-01	16	16	0	0	0	0	0	0	0

# Yield of First Two Wafer Lots



Lot Averaged Yields: Z39992 = 14.09% Z39993 = 29.35%

It's clear that there are large variations in the quality of wafers, even within one fab lot.

The promising note is that the yield of lot Z39993 is much better than any of the pre-production lots. With the exception of 3, all wafers tested in that lot are at or above the contract minimum yield of 26%.

Seven wafers have not yet been tested, 2 from Z39992 and 5 from Z39993.

## **Yield Improvement**

The yield of the first two lots is both encouraging and frustrating.

Many of the wafers exceed the 26% yield by a substantial amount and demonstrate that good yields are possible. These yields are much higher than what we saw in the pre-production wafers.

At the 5-Jul meeting, ATMEL told us of several changes in their line to improve yield. They seem to be working.

At the same time, some wafers have miserable yield. Poor consistency in process control?

ATMEL is also in the process of qualifying a new sub-contractor to grow the epitaxial film on the SOI wafers.

Sample lots in 2000 and Spring-2001 showed much better yield with wafers from this new sub-contractor.

A final qualification lot is now being tested at RAL and UCSC to confirm the better yield. A few modules were built with chips from this new sub-contractor. We are studying the results of these tests now.

If this qualification is successful, ATMEL will switch to this new subcontractor for all production wafers after they have delivered approximately 200 production wafers from the old sub-contractor.

## Wafer Testing

Three test systems are qualified at CERN, RAL and UCSC. A fourth at UCSC is also available with its additional probe station on order.

Test time is now approximately 9 hours/wafer

Changes to test algorithm are planned to further reduce test time and to add some tests of I/O signals.

These changes will be qualified in the next 2 weeks.

Test time should be reduced to ~4.5 hours/wafer based upon timing trials.

Testing 2 wafers/day/test site is possible with a split shift of operators.

This has been successfully accomplished at UCSC for 1.5 weeks to test 16 wafers.

This will be further facilitated by reducing the test time down to < 7 hours/wafer.

# **Production Plan for Wafer Orders and Deliveries**

Week #	Date	Raw Wafers	Fabrication	Wafers Received	<b>Expected Yield</b>
	(last of Month)	Released	Released	by CERN	at Wafer Test
40	Sep-00	520			
		520			
31	Jul-01	675	520		
35	Aug-01	675	520	35	11.00%
39	Sep-01	675	520	35	11.00%
44	Oct-01	950	520	205	15.00%
48	Nov-01	950	675	405	15.00%
52	Dec-01	1,105	675	520	26.00%
5	Jan-02		675	520	26.00%
9	Feb-02		950	620	26.00%
13	Mar-02		1,105	675	26.00%
18	Apr-02			675	26.00%
22	May-02			675	26.00%
26	Jun-02			875	26.00%
31	Jul-02			1,105	26.00%

**Cumulative Monthly Plan for wafer orders and deliveries:** 

# **Production Plan for Chip Availability**

Actual chip availability is highly dependent upon actual yields.

This is a conservative plan based upon yields assumed in previous Wafer Delivery Plan.

Week #	Date	Total Delivered Chips						
	(last of Month)	Japan	UK-B	LBNL	Scand.	Forward		
44	<b>Oct-01</b>	411	446	0	77	0		
<b>48</b>	Nov-01	411	460	0	77	0		
52	<b>Dec-01</b>	783	683	93	644	0		
5	Jan-02	1,188	1,291	<b>498</b>	1,615	0		
9	Feb-02	1,695	2,052	1,005	2,883	0		
13	Mar-02	2,202	2,622	1,512	4,064	0		
18	Apr-02	2,836	3,572	2,146	5,268	0		
22	May-02	3,631	4,333	2,941	5,658	0		
26	Jun-02	4,949	5,650	4,259	5,658	0		
31	Jul-02	6,047	6,474	5,357	5,658	2,581		
35	Aug-02	6,925	7,133	6,236	5,658	5,436		
39	Sep-02	7,804	7,691	7,114	5,658	8,393		
44	<b>Oct-02</b>	8,487	7,691	8,420	5,658	11,577		
<b>48</b>	Nov-02	8,487	7,691	9,282	5,658	14,669		
52	Dec-02	8,487	7,691	9,282	5,658	17,305		
5	Jan-03	8,487	7,691	9,282	5,658	21,258		
9	Feb-03	8,487	7,691	9,282	5,658	25,212		
13	Mar-03	8,487	7,691	9,282	5,658	27,321		
18	Apr-03	8,487	7,691	9,282	5,658	27,551		

**Cumulative Monthly Plan for chip availability:**