Wafer Screening Status and Update on Test Sequence

- Sequence of Tests
- Fast Pipeline Test
- Analogue Tests
- Digital Tests
- Testing Time Reduction
- I/O Signal Tests

LBNL ASIC Tester

Testing sites

LBNL ASIC Tester

- The tester measures values and tolerance ranges of all critical IC parameters, including DC parameters, electronic noise, time resolution, I/O signal levels and clock timing.

- The tester is controlled by an FPGA (ORCA3T) programmed to:

  - interpret VME commands and generate the bit-streams to be sent to the ABCD3T

  - interpret the bit-stream produced by the ABCD3T during the analog calibration procedure and store the histogram of hits in a dedicated memory chip on the board

  -store a test vector and the simulated response (simulation vector) of the chip in a memory on the board, to send the test vector to the chip, compare the chip response with the simulation vector and provide the result of the comparison. This procedure is used for digital testing of the chip

The data between the VME board and the probe card are transmitted as differential signals. To characterize signal amplitudes and phase margins, the tester utilizes pin-driver, delay, and DAC chips, which control the amplitudes and delays of signals sent to the IC. Two intermediate boards have been designed and built to provide:

  - High current pin drivers for inputs with variable signal level

  - Signal delays

  - Window comparators discriminating on the upper and lower output signal levels

  - Dedicated ADCs to probe the internal ABCD3T parameters; power consumption and feedback control of voltages supplied to the chip and ambient temperature of the pin driver board.

A probe card has been designed specifically to reduce pick-up noise that can affect the analog measurements.

The system can operate at frequencies up to 100 MHz to study the speed limits of the digital circuitry before and after radiation damage.

Testing Sites

UCSC – RAL – CERN

- All testers operational since April/June

  CERN's wafer screening facility is temporarily not available

  Tester about to be re-installed at CERN or at a company if decision to outsource wafer screening

- Hardware fully working
  - New revision or updates of boards (VME, intermediate boards, single-chip-test card) produced over the last few months are used at the sites, including spares
  - Additional probe cards under fabrication

- Correlation studies completed by the time of PRR (July 4)
- Production wafer testing started

- Online software stable but plan to implement new tests and changes to reduce testing time
- Offline software operational but work in progress to make it available on the ATLAS cluster

  Software maintained in CVS

  Vitaliy Fadeyev (LBNL) coordinator for Online and Bill Murray (RAL) for Offline both for Database (implementation of ASIC definition tables in SCT Database in progress).

Testing Sites: RAL

Testing Sites: UCSC

Sequence of Tests

1. "DEAD/ALIVE"
   Configuration Register R/W test. Skip chip if test fails
2. "FAST Pipeline" ⇨
3. Power Consumption measurements
   Measured separately in analogue and digital parts of the chip for nominal speed, bias, trigger rate and hit occupancy conditions, MASTER and SLAVE mode
4. Analog Test for Gain, Offset, Noise characterization
5. Analog Test for the Trim DACs linearity
6. Analog Test for the Trim DACs Range ⇨ (4–6)
7. Strobe Delay Scans
   To assess the "speed" of the chip, also used to choose the Strobe Delay parameter for a given lot of wafers
8. DACs (Threshold, Preamp, Shaper) linearity scan
9. Digital Tests ⇨
10. I/O Signals Phases ⇨
11. I/O signals Voltage Levels ⇨

To speed up the Wafer Screening and to qualify the chips better, tests (10), (11) will be introduced and test (9) modified after screening the initial batch of 35 wafers.

“Fast Pipeline” tests

- ➔ The purpose is to scan/test the digital pipeline.
- ➔ Similar to some of the test vectors, but faster and provides more information. Uses analog scans functionality of the tester, to
  - ➢ Set the chip in the right state
  - ➢ Send bunch of triggers interspersed with proper command

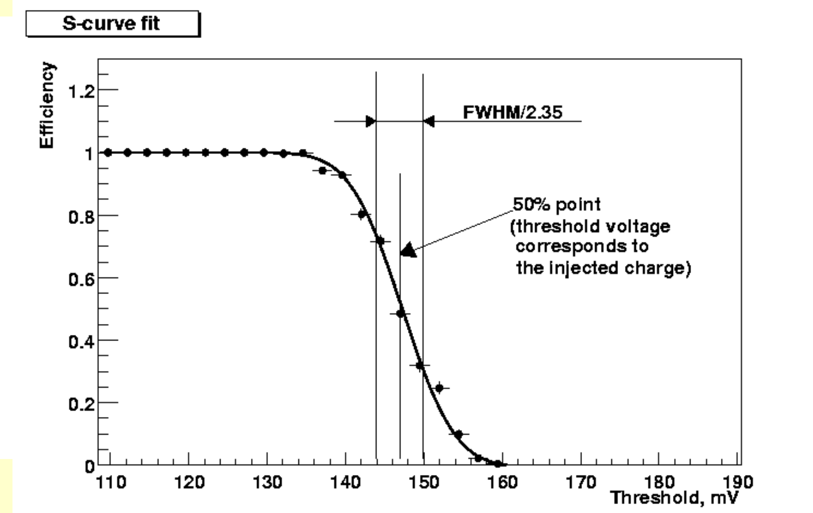
    Static Pipeline Test: Calibration Pulse + triggers

    Dynamic Pipeline Test: Latch the data from “Pulse Input Register” command
  - ➢ Decode the data-stream in firmware, store the hits for individual channels in VME board memory and read them out after the scan.
- ➔ Different masks (“1111...”, “0000...”, “0101...”, “1010...”) and proper trigger-to-trigger delays are used to thoroughly scan the pipeline.
- ➔ Information on the channel-by-channel basis (if stuck low, stuck high, overly efficient, or has some “funny” behavior).
- ➔ Online selection (skipping the rest of the tests) is possible with cuts of varying severity, but not planned to be used yet. We reserve this option for the case of low yield, and/or the need of larger wafer throughput.
- ➔ The tests are very fast (less than a second per chip), but can only be used at 40 MHz.

Analogue tests

Gain, offset and noise characterization

To determine gain, noise and discriminator offset for each electronic channel.
Threshold scans (7.5 mV step) for four different input charges{2.5, 2.875, 3.625, 4.0} fC
The input transistor current and shaper current are set to nominal values (30 µA, 220 µA)
Frequency at 40 MHz, Chip MASTER&END
Four S-curves per channel are fitted to a complementary error function.
From the 50% points the gain curve is extracted and fitted to a straight line.
The gain and the offset are taken as the slope and offset of the linear fit respectively.
The electronic noise is obtained from S-curve fit.



Characterization of the TRIM DAC's

Trim DAC of 4-bit resolution to compensate for chan-to-chan variation of the discriminator offset.
TRIM DAC Setting: 0001/0010/0100/1000/1111
TRIM DAC RANGE: 00
Fixed calibration pulse (2.5fC)
Threshold step 7.5 mV

Characterization of the TRIM DAC range

Two bits range to cover the offset spread.
Scan at one TRIM DAC value (1000), one calibration charge (2.5fC), and 7.5 mV threshold step.
TRIM DAC RANGE = {01, 10, 11}

Digital Tests

We test the digital functionality of the chip with "test vectors". Each of them is a pair of a predefined sequence of input data and the expected chip response. The comparison of the "real" chip response with the expectation is done on the fly in the FPGA. Only the results ("yes/no") are read out during the production testing.

Both Vdd and Frequency are scanned for each test vector:
- Vdd from 3.3 to 4.1 V in steps of 0.1 V,
- Frequency from 40 to 90 MHz in steps of 10 MHz.

Test Vectors description courtesy F. Anghinolfi. Also shown are stimulated I/O lines. Each TV has the resetB input line de-asserted soon after the beginning (not indicated in this Table).

TV	Stimulated Input Lines	Affected Output Lines	Purpose/Description
w1test	com0	datalink	Configuration register Write/Read test. Bits 0 thru 10 are scanned.
w2test	com0, id0, id1, id2, id3, id4	datalink	BC counter test (all 8 bits are checked). ID address bits test. Overflow function and error code test.
w3test	com0	datalink	Data Compression Logic tests with random channel mask. Having "one"s in different bits of the 3-bit hit discription.
w4_fulltest	com0,	datalink	Dynamic digital pipeline test. Masks ...1111..., ..1010..., ..0101..., ..0000... Accumulate function.
w4_2testcom1	com1, select (const)	datalink	Dynamic digital pipeline test. Mask ..1111... Accumulate function.
w5test	com0, tokenin0, tokenin1, datain0, datain1	datalink, tokenout0, tokenout1, dataout0, dataout1	Data/tocken bypassing circuitry test.
w6test	com0	datalink	Static digital pipeline test. 4 masks. Accumulate function test.

Reduction of Screening Time

Digital Tests

The digital tests are currently taking the larger fraction of the screening time.
To reduce the testing time, we are going to introduce the following changes (after the first batch of wafers):

→ merge 4 different "W4_2Xtestcom0" test vectors (with 4 different masks) into single "W4_2fulltest", thus economizing on the chip initialization procedures

→ high-frequency scans at Vdd = 3.7 V only (used to do that for all Vdd scan values)

→ change the number of times each test vector run at a given {Vdd, Frequency} value from 100 to 10.

Analogue scans

We have established the dependence of the precision of the measured values of noise, gain, offset, and trim slope on the repetition parameters using analytic and Monte Carlo techniques and verifying that with tests.
We agreed to use 200 events per threshold point.

I/O Signals Tests

Tests of the chip signal levels and phases by running test vectors utilizing these signals and varying the conditions. The working range is exceeded when the test vector efficiency is below 100%.

Test Type	Scanned Parameter	Extracted (Output) Quantity
input phases	input signals delays	The value (and its error) of the extra time delay of the signal when the ABCD is having a signal latching problem.
output phases	output signal delays	The value (and its error) of the output signal time delay wrt the input clock.
input levels	swing of the input differential signals	Minimal value of the swing at which the test vector still works.
output levels	window comparators thresholds	The signal swing.
clocks duty cycles	duty cycles of the clocks supplied to the ABCD	The Minimal and Maximal working values of the clock duty cycle.

- The tests are “new” -- these quantities have not been measured before
- These tests are possible due to the special features offered by the “new” tester.
- We plan on imposing only very loose selection on the measured parameters
- The extracted information should be mostly useful for building the hybrids and manufacturing process control.
- More comprehensive characterization of the chip

I/O Signals Levels

Input Levels

- The ABCD3T input differential signals are provided by the pin driver chips (Connector Board).
- Two chips are supplied for each signal, e.g. one for COM1 and one for COM1B sides of the COM1 input.
- Each pin driver chip has two input voltages, set by DACs, which define the high and low voltage levels for the output signal (and correspondingly, the ABCD3T input signal swing).
- We set all other signals at nominal conditions and scan the input swing by changing the pin drivers input voltages supplied by DACs.
- We run a test vector, for which the signal changes its state multiple times.
- The voltage values, for which the test vector is 100% efficient, define the signal working range for the chip.

Output Signal Levels

- Each differential output signal of the ABCD3T goes through a diff. amplifier and a window comp. (WinC).
- A signal passes through the corresponding WinC if its high level is above the WinC thresholds and its lower level is below the WinC thresholds.
- We run a test vector which toggles the output signal level and scan the WinC thresholds, with both thresholds set to the same value.
- We expect that the TV efficiency would have a plateau centered at the differential amplifier voltage level (1.2V for datalink/LED and 2.0V for all other signals).
- The test vector efficiency transitions between 100% and 0% efficiency indicate the high and low signal voltage levels.

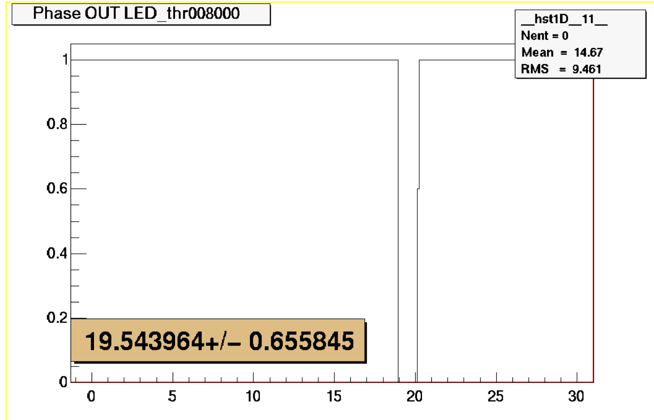
I/O Signal Phases

Input Signals Phases

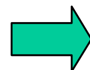
Each of the input signals passes through a delay chip, therefore there is a capability to scan its phase wrt clock. For each signal, the delay is scanned while other signals (including clocks) are kept at nominal conditions.

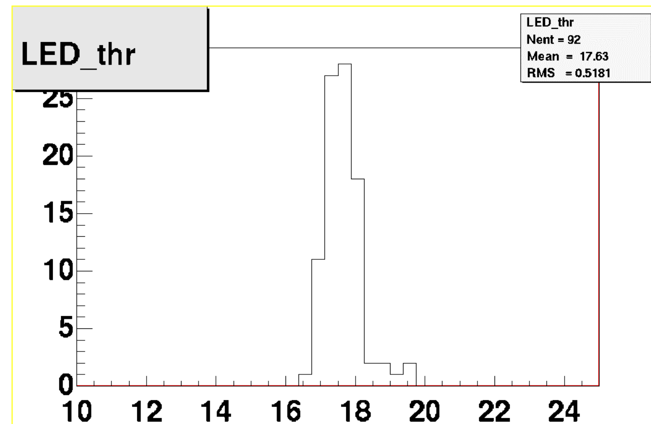
Output Signals Phases

All the output signals are passed through a register. The latching clock for this register can be delayed. The delay range is the same as for the input signals delays. This feature is used to find the phase of an output signal relative to the clock. When the phase is zero, there is an efficiency loss for the test vector.



TV efficiency versus the delay between the datalink/LED latching clock and CLK0 [ns] for a single chip. The position of the efficiency dip indicates the datalink/CLK0 relative phase.





Distribution of datalink/CLK0 phase, in [ns], for wafer Z37277/W24. Only digitally good chips are considered in this histogram.

Summary

- The tester has been performing well during the pre-production and beginning of the wafer production testing.

- Hardware is working reliably
  All sites have updated or final revision of boards and spares

- The sequence of tests includes, besides the standard tests:
  - The "Fast Pipeline" test which in the case of low yield, and/or the need of larger wafer throughput could be used to reduce screening time
  - The I/O Signals Tests for more comprehensive characterization of the chip

- Plan to implement several changes that will speed up the wafer screening.
  Tested 1 wafer with smaller analogue and digital repetition values, testvectors combined, high-frequency scans at Vdd (even including the new I/O tests) the wafer screening time was reduced from ~10 hours to 4 hours 20 minutes.
  The goal is < 7 hours/wafer

- Online S/W is stable but new version is going to be used for the next batch of wafers after validation of new tests on current wafers

- Offline S/W to be centralized at CERN and Database implementation in progress