ASIC Test System for SCT

Alessandra Ciocio
Lawrence Berkeley National Lab

- Overview
- Boards Functionality
- Measurements and Performance
- Future Development
- Software
- Schedule

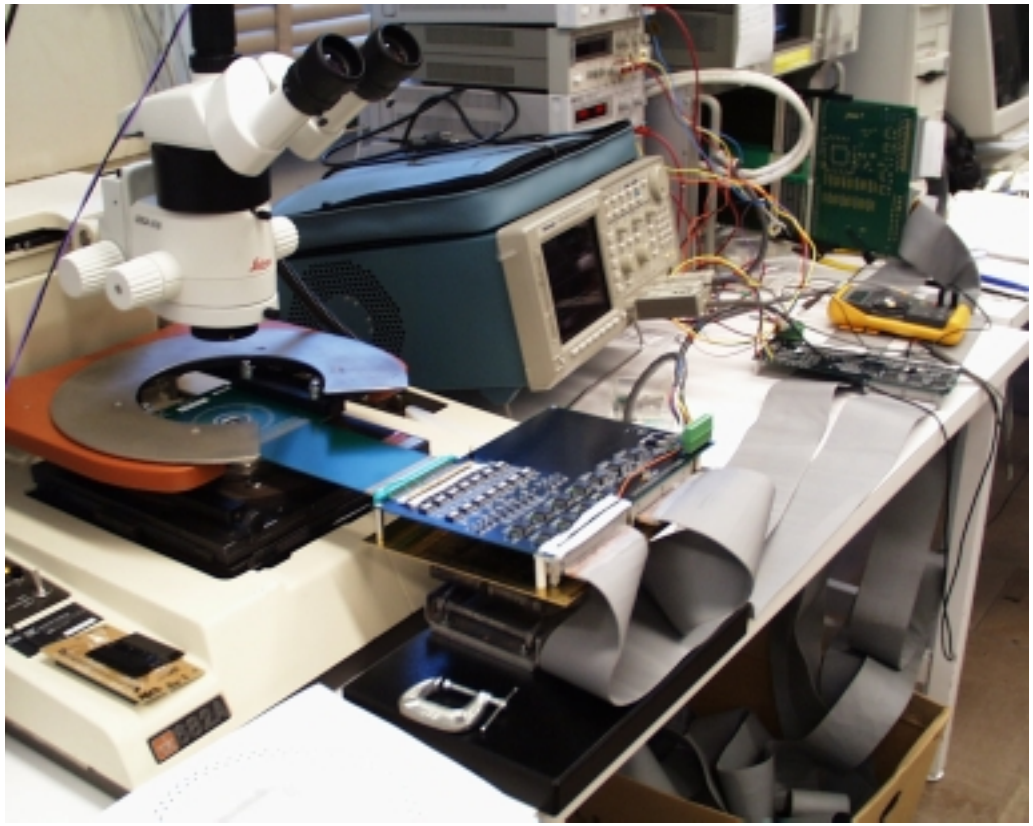
Overview

Original LBNL design (Hubert Niggli)
Currently under debugging and production at LBNL by:

Alessandra Ciocio, Naim Busek,
Chinh Vu, Thorsten Stezelberger,
Gil Gilchriese, Carl Haber,
Francesco Zetti

George Zizka, Helen Chen

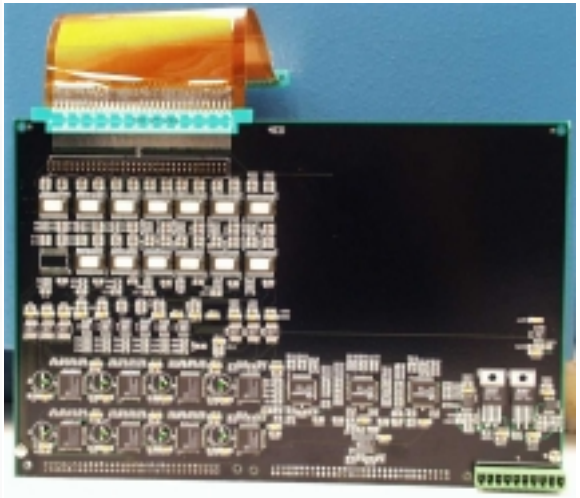
in collaboration with UC SantaCruz
Tim Dubbs, Alex Grillo, Abe Seiden,
Ned Spencer

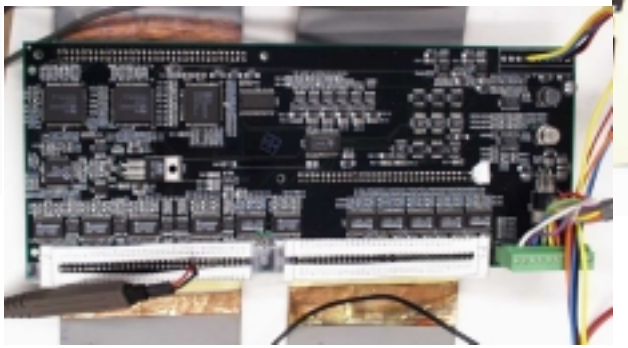


Overview

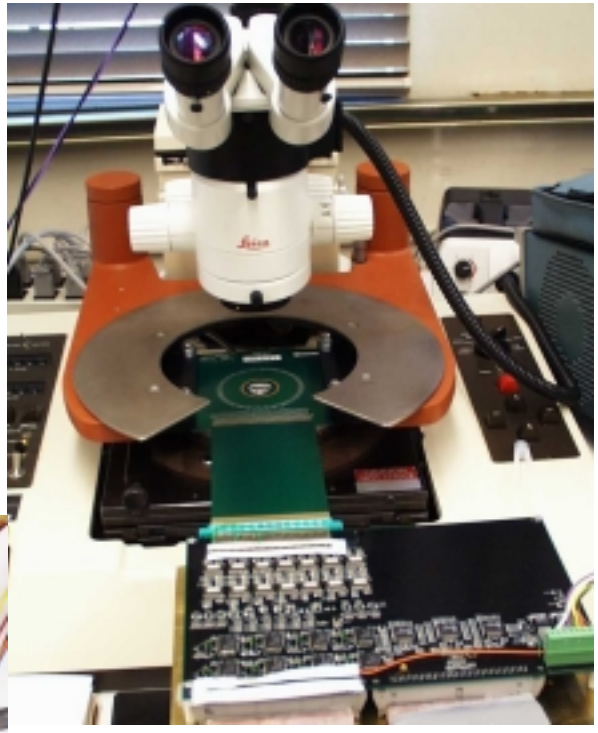
VME Board

Pindriver board(s)



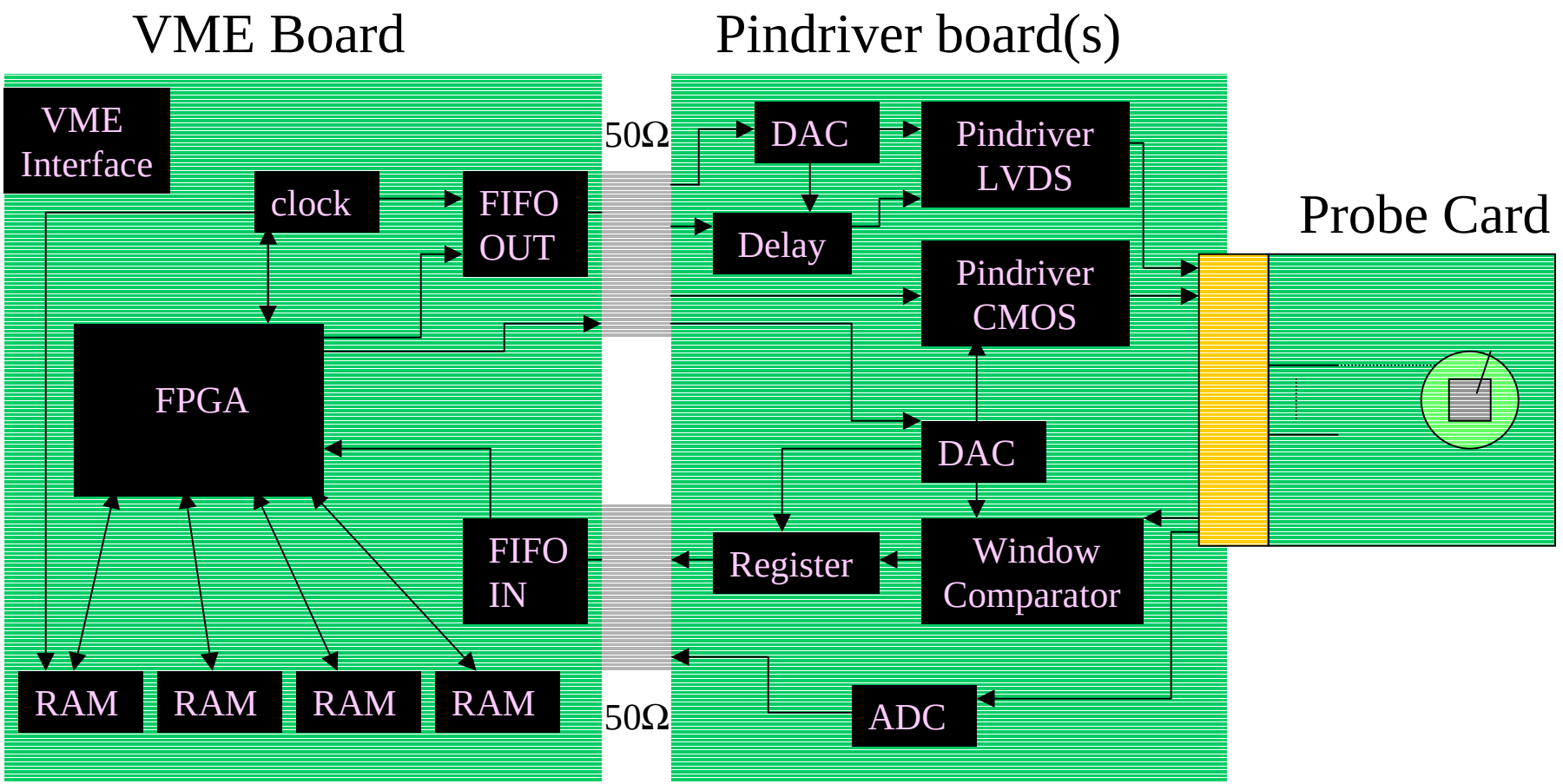


Probe Card



http://www-atlas.lbl.gov/strips/tester/

Overview



All operations are programmed here in the FPGA using VHDL.

Allows to adjust amplitude and delays of the signals within a range to test functionality of ABCD by feeding them through pindriver and delay chips.
DACs allow to vary parameters.
Signals from ABCD go through window comparator.

Boards Functionality

VME board

FPGA (Orca device-Lucent Tech)
- Functionality of FPGA is determined by internal configuration RAM
- Configuration data resides externally in 2 PROM
  - RAM is loaded at power up and under system control
  - Power-on-reset circuit is trigger when power is applied (25 ms delay until operating VDD is reached)
- Programmable in VHDL (Mentor Graphics)

FIFO
Input and Output

Memory (MCM69P819)
2x4 array 256K x 18 bit fast static RAM
histogram data, sim vector, testvectors

VME Interface

Frequency: 40MHz for all components but higher frequency can be used for front-end FIFO and ABCD

On-board comparison of chip response to testvectors with Verilog simulation. The simulation vector is stored in the sim vector memory. The result of the comparison is one bit in the FPGA status register.

Boards Functionality

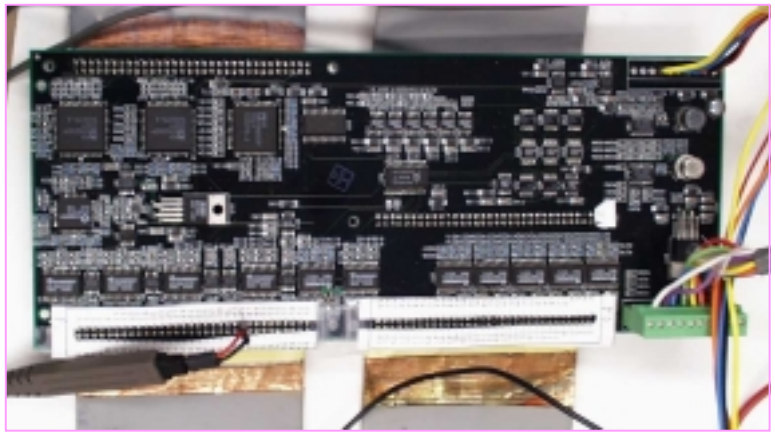
VME board

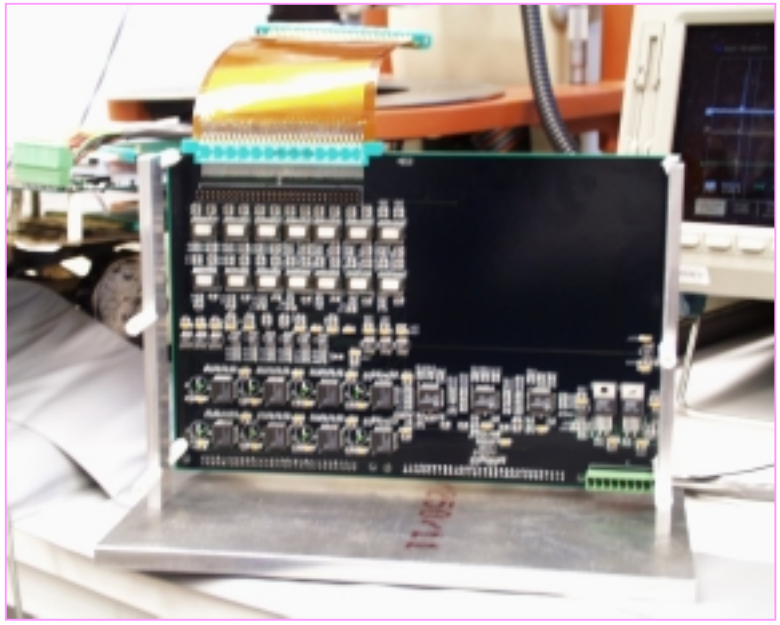
Functionality of the VME board *(what the VHDL code does)*:

- Create serial bitstream to load registers in the ABCD (or all if module)
- Create serial bitstream to load DAC's to set supply voltages VCC and VDD to the ABCD on the support card (module) or pindriver board (if ASIC testing)
- Read back ADC data
- Set frequency of the clock synthesizer
  (or the main clock must be used for the FIFO's also by setting the 4dip switches)
- Send triggers to one ABCD (ASIC testing) or to a module
- Read data back
  Data is received via the resync FIFO
- Decode the serial data
  Data is decoded in the "serial to parallel decoder" blocks
- Create histograms of the data and write them in memory

Boards Functionality

Pindriver Board(s)





Pindriver

VME interface board

Signal level translators:

LVPECL⟶ECL and PECL⟶TTL

DACs

Delay circuit

ADC chip

VCC VDD circuitry

Concard

Probe card interface board

Pindriver chips for LVDS and CMOS signals

DACs

Window comparator

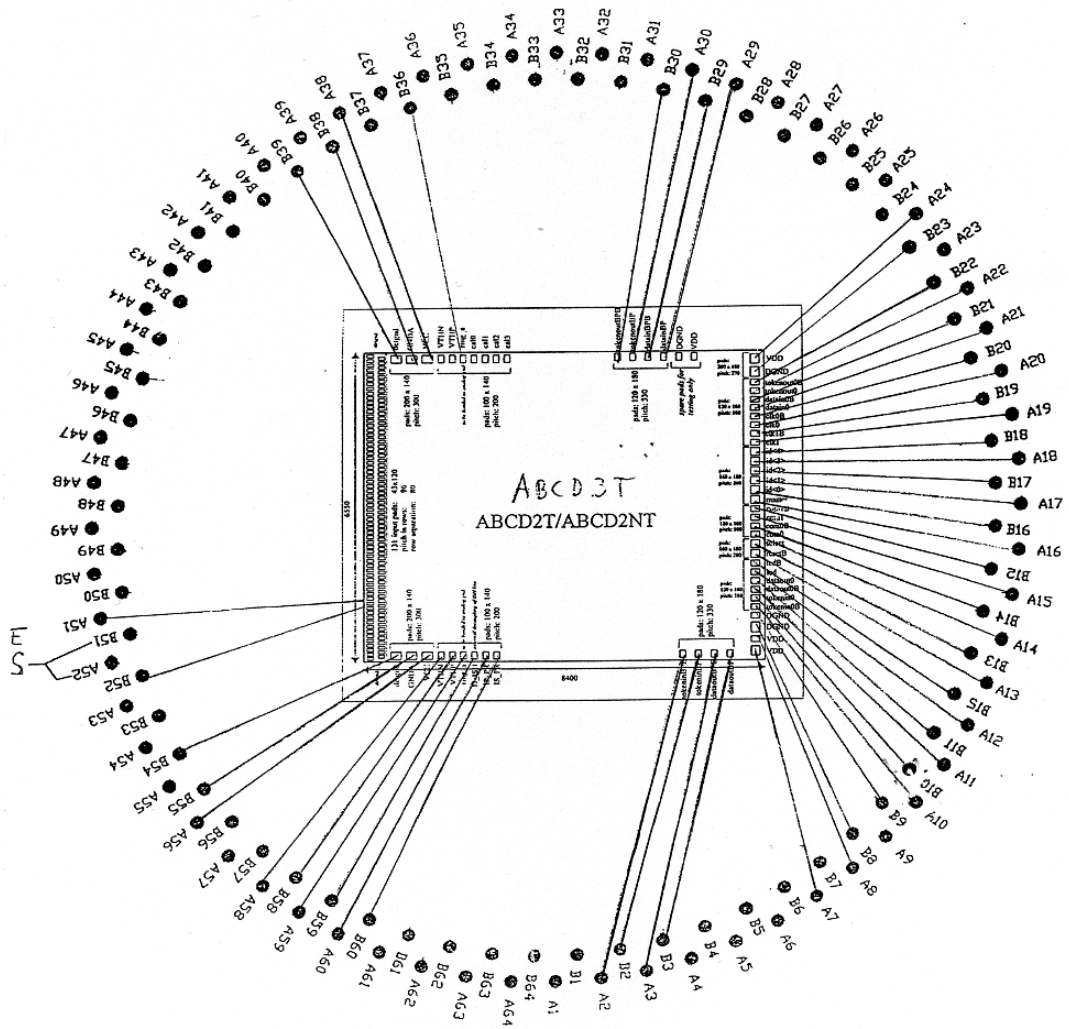
Output Register

All cables are 50 Ω

VME⟶Pindriver⟶ Concard

Concard connects directly to probe card
or through ~10cm Kapton

Boards Functionality



Probe Card

4-layers matched impedance standard PC board

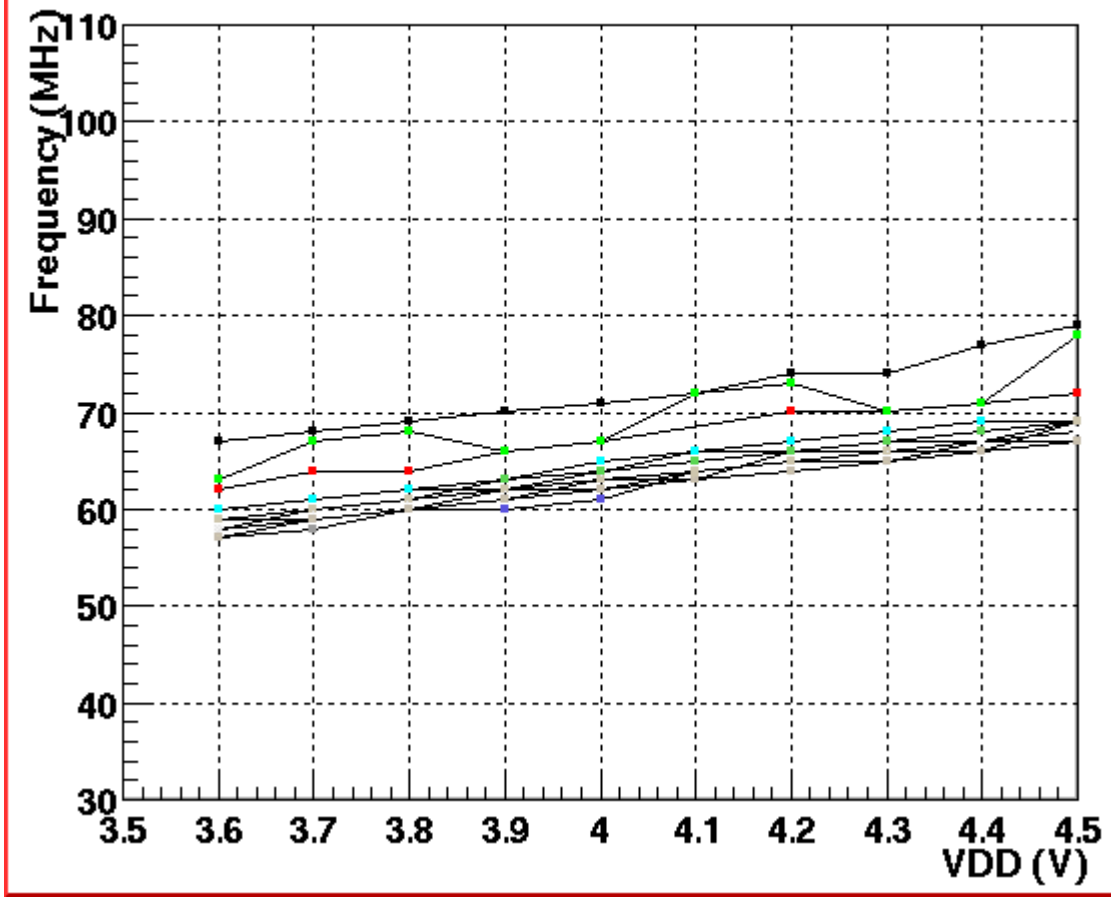
53 Probes

Signals are terminated close to the probes

Similar probe card for ABC operated at higher frequency

Boards Functionality

ABC testvectors



Measurements and Performance

Threshold scan

ABCD on hybrid (old module setup)
4 threshold scans at 1.3, 2., 2.3, 3. fC
each threshold scan of 48 threshold steps, 500 events/step.
the measured noise (from a quick calculation) of the order of 500 electrons
time to do a complete scan of one calibration line (6.2 seconds)

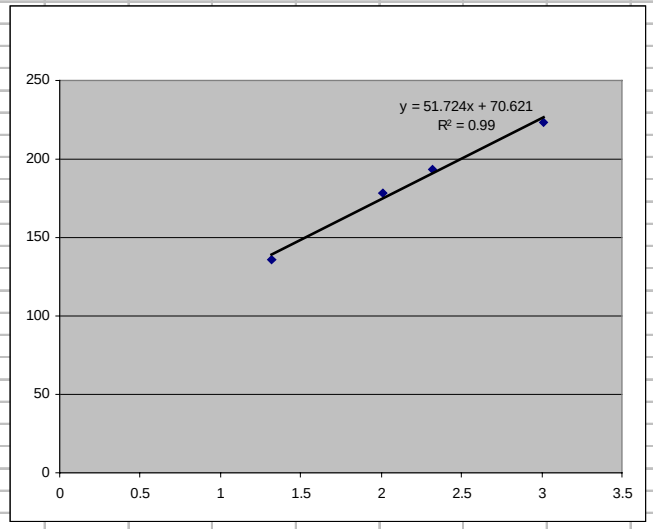
ABCD on test board plugged on concard (using the new pindriver boards)
4 threshold scans at 1.3, 2., 2.3, 3. fC
each threshold scan of 48 threshold steps, 100 events/step.
the measured noise (from a quick calculation) of the order of 800 electrons
time to do a complete scan of 4 calibration lines (8 seconds)

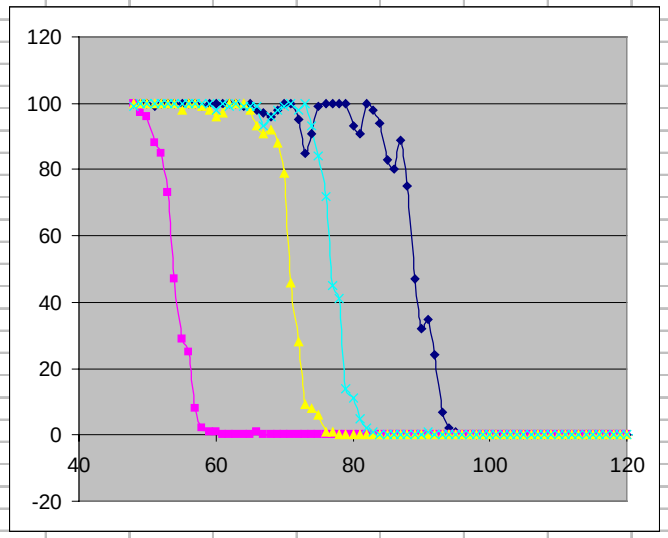
ABCD single die on Probe Station (using new probe card and pindriver boards)
Digital part responds well. Analogue still shows some parasitic pickup.
Under debugging.

Measurements and Performance

ABCD on test board plugged on concard

						charge			
hex	calib (bits)	calib (fC)	thresh 50%	thresh 50% (mV)		15	20	25	30
			+- 0.5						
15	21	1.317647	54	135.5294		12% point			
20	32	2.007843	71	178.1961		57.000	73.000	80.000	93.000
25	37	2.321569	77	193.2549		88% point			
30	48	3.011765	89	223.3725		51.000	69.000	74.000	87.000
						width			
						2.532	1.688	2.532	2.532
						width in (mV)			
						6.354	4.236	6.354	6.354
				gain		width in (fC)			
				51		0.125	0.083	0.125	0.125
						width in (e-)			
						777.696	518.464	777.696	777.696





800 electrons
8 seconds/S-Curve

Future Development

Start close collaboration with CERN/RAL
Meeting May 29 to discuss convergence to one system and compatibility with all probing sites
How to get ready for August 14

- Mechanical issues
  - How to connect pindriver board to a different probe station geometry
  - Study the possibility of a longer cable (50 cm) or redesign pindriver board and put window comparator on probe card to improve analogue signals
  - cooling of pindriver board
  - header pins on probe card (eliminate Viking connectors)
- Complete hardware debugging
  - Need to perform speed test
  - Achieve at least 60 MHz performance
- Produce system for UCSC, CERN, RAL
  - Besides VME and Pindriver supply also a single chip test board to allow initial testing/debugging without using probe card
- Documentation

Software

Test software to perform Threshold Scan runs at LBNL with new hardware

PC/WNT, application MSD (C++), controlling VME using NI-MXI/PCI interface

Library for VME/FPGA/Memory controls/commands

CERN test software

PC/W95, Visual C++, controlling VME using NI-MXI/PCI interface

Libraries for threshold scan, digital test, trim DAC, DAC linearity,

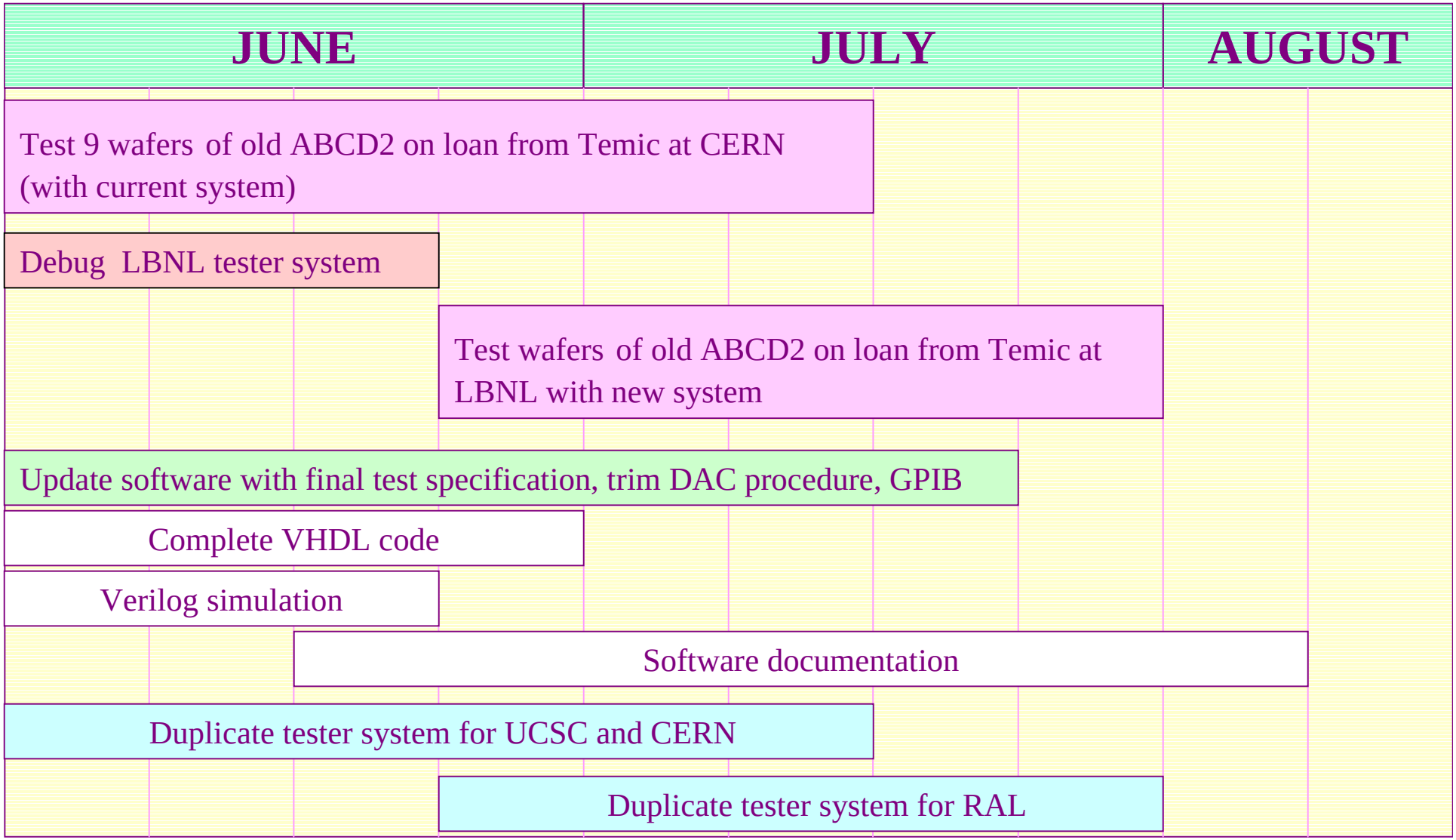
Window, configuration, test, GPIB controls (C++ classes)

- VME/FPGA library will merge into CERN test software (Carlos)
- CAFÉ-P + ABC test spec lists will be compared with current ABCD/CERN list (Tim, Ian, Marcus)
- Verilog simulation for testvectors (Francis)
- FPGA/VHDL is almost complete (needs ADC procedures) (Thorsten)
- Documentation (Carlos, Sandra)

to keep in mind:

- Modularity to allow to be used with different hardware setup and module test/burn-in
- Agree on a test specification to satisfy Temic requirements for guaranteed yield

Schedule


JUNE
JULY
AUGUST
Test 9 wafers of old ABCD2 on loan from Temic at CERN (with current system)
Debug LBNL tester system
Test wafers of old ABCD2 on loan from Temic at LBNL with new system
Update software with final test specification, trim DAC procedure, GPIB
Complete VHDL code
Verilog simulation
Software documentation
Duplicate tester system for UCSC and CERN
Duplicate tester system for RAL