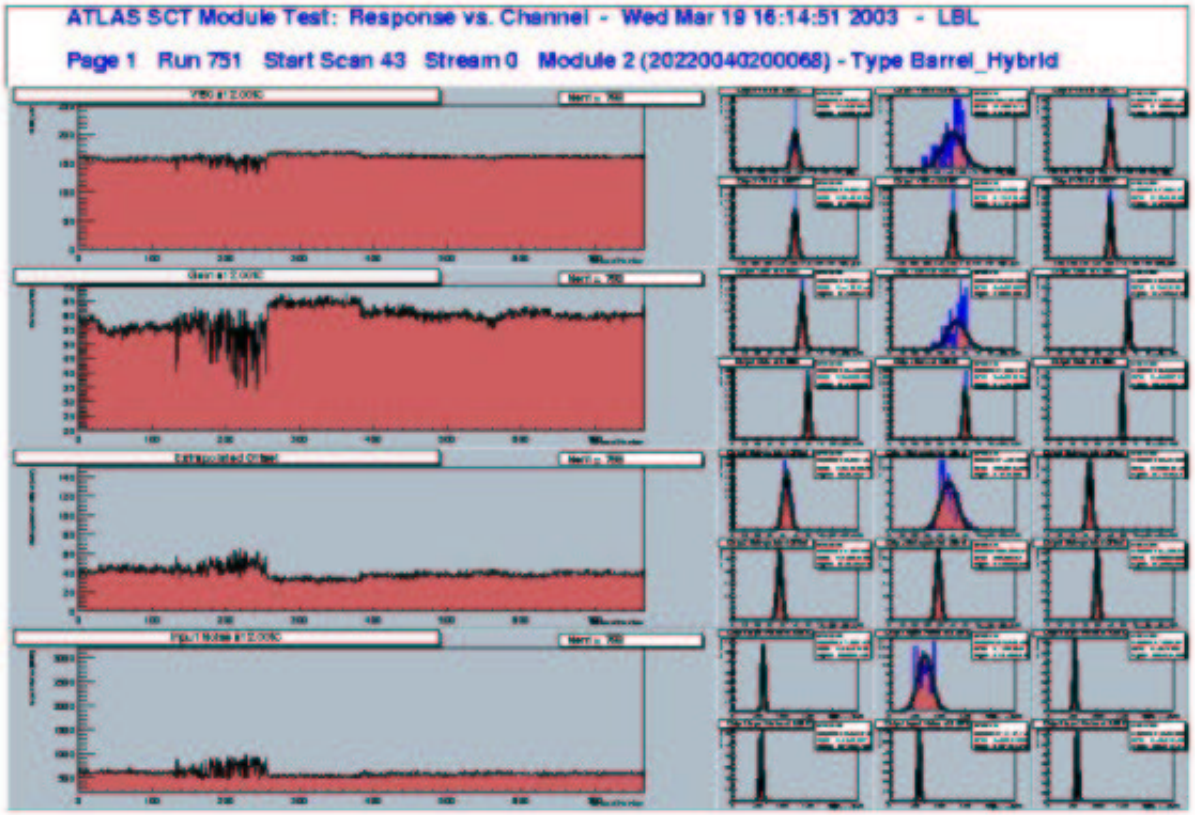
LGS Study

A study of the Large Gain Spread (LGS) effect was conducted in numerous ASIC's to better understand the causes, effects, and possible solutions



Areas of the Study

- ISh and Vcc
- Icc
- FE DAC's

Ish/Vcc Study

Vcc was stepped between 3.4V and 3.7V (in 0.1V increments) and for each of these settings, the shaper current was set at 20, 25, 30 (nominal), and 35 micro Amps.

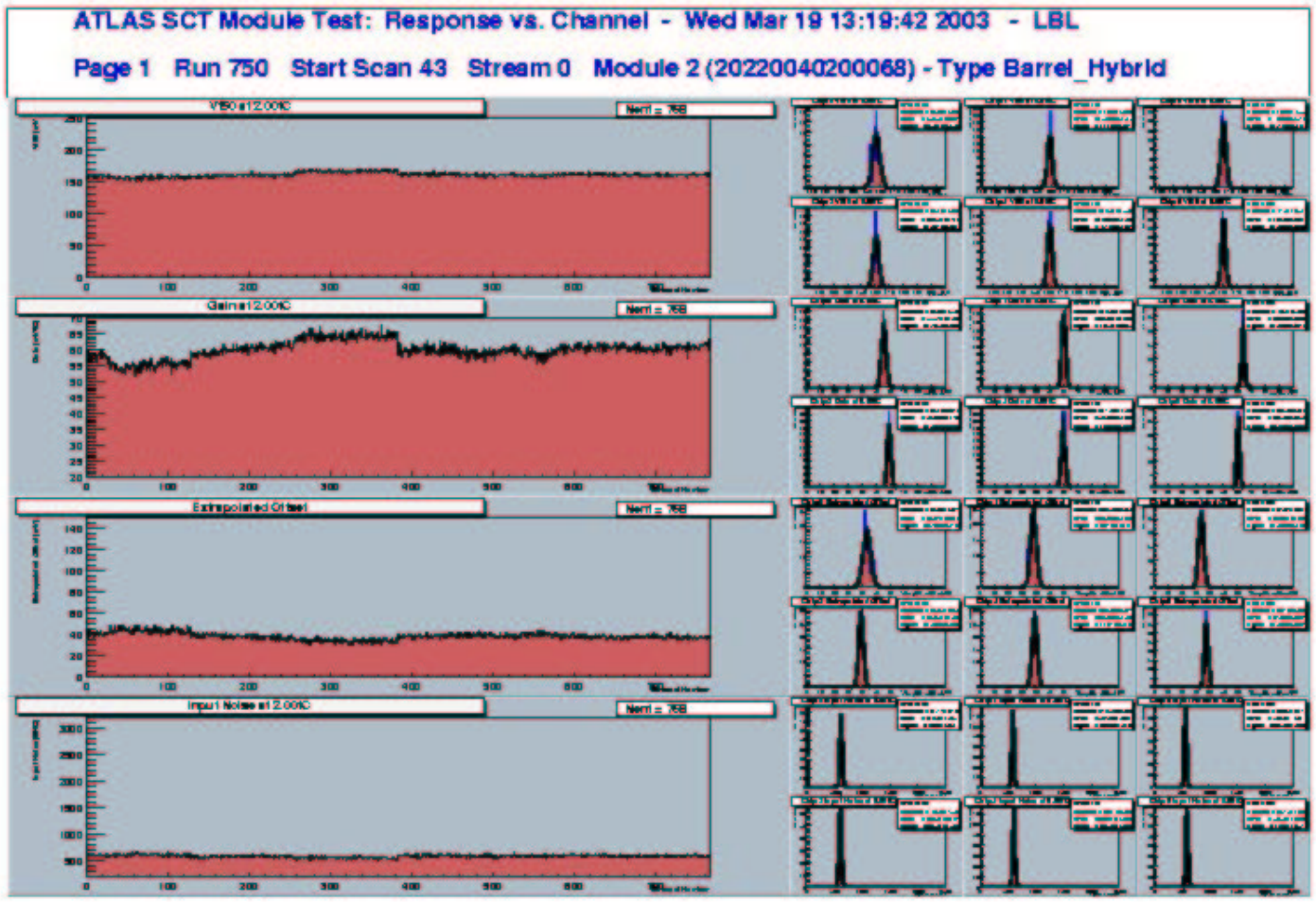
For chips with LGS the gain becomes regular for Vcc > 3.6V
or at Vcc=3.5V (nominal setting) and Shaper current ISh=20 μA

Tests were done at room temperature and at 0° C (where the spread is worse).
At room temperature, Ish=25 is already enough to cure the large spread

Test were performed on 4 different hybrids and similar results were obtained in all cases

http://www-atlas.lbl.gov/strips/modules/production/lgs-study/

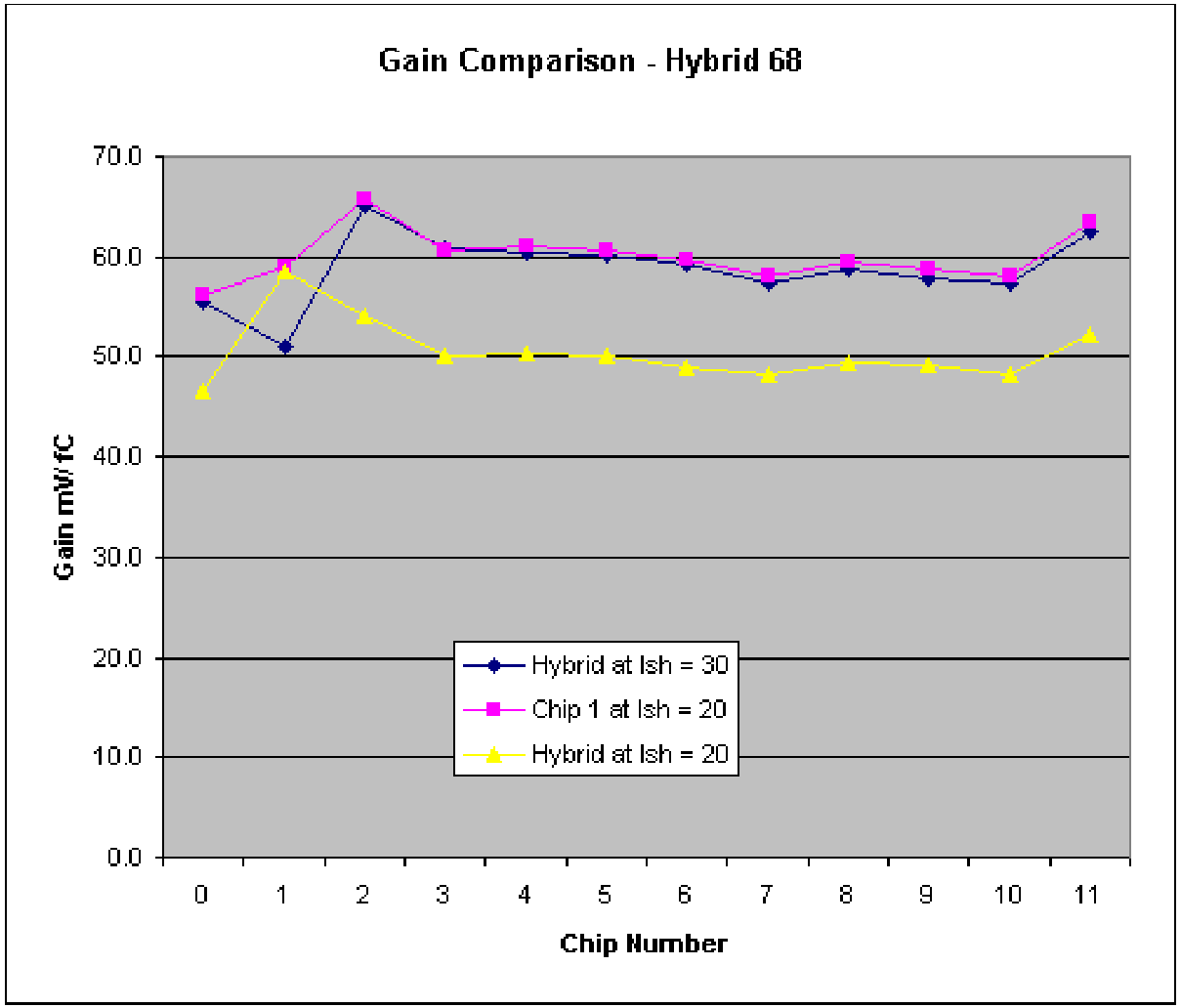
Ish/Vcc Study - ISh = 20 μA
(for chip with LGS)



Vcc=3.5V and ISh=30 μA for all chips

except ISh=20 μA for S01 (which has LGS at ISh=30 μA)

ISh/Vcc Study – All chips of one hybrid



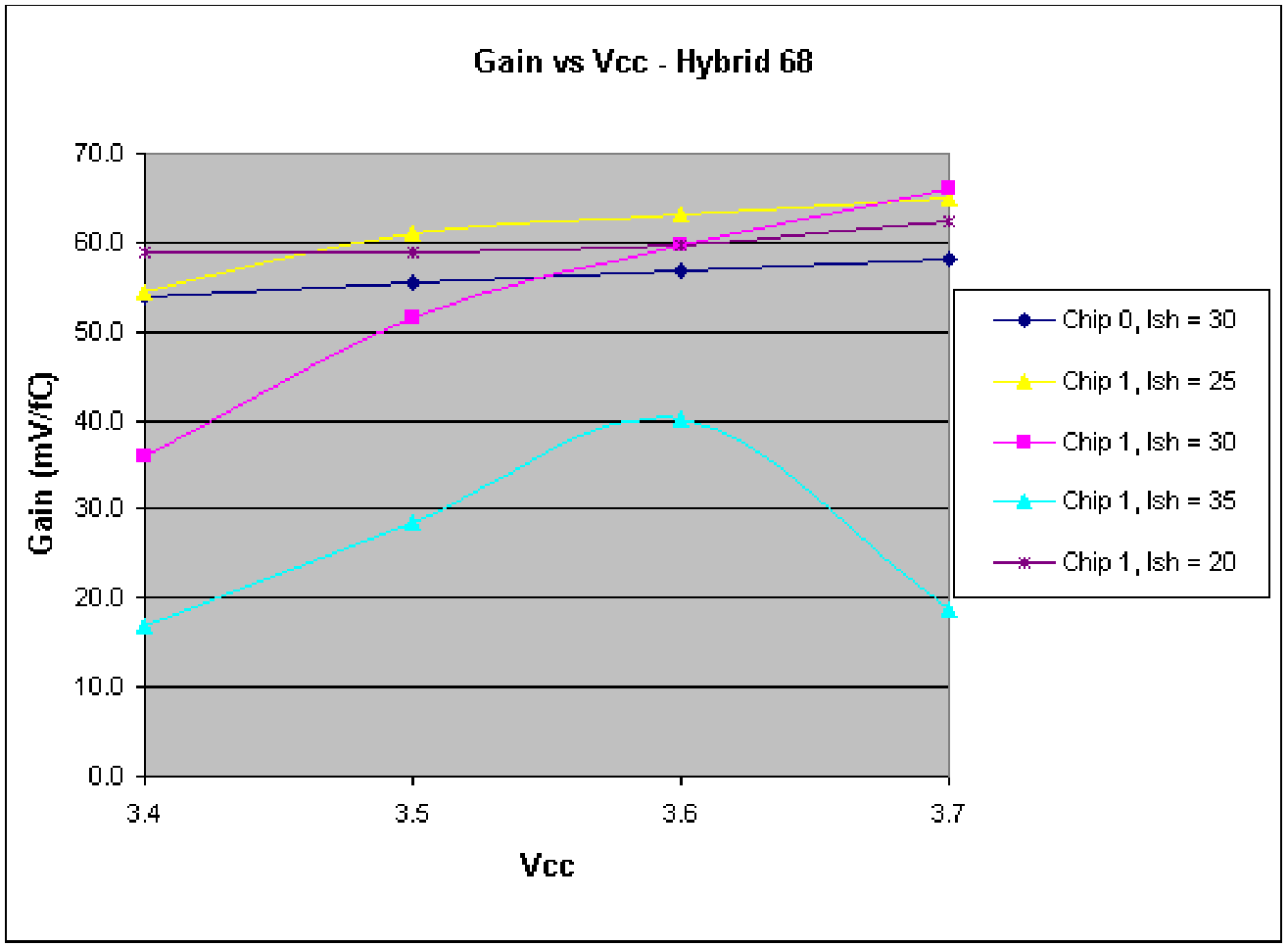
Vcc=3.5V

Comparison between all chips of one hybrid for different settings of Ish (S01 has LGS)

When Ish=20 only for S01 overall gain is comparable

All chips at Ish=20 gain is very low

ISh/Vcc Study - Gain vs VCC and several ISh settings



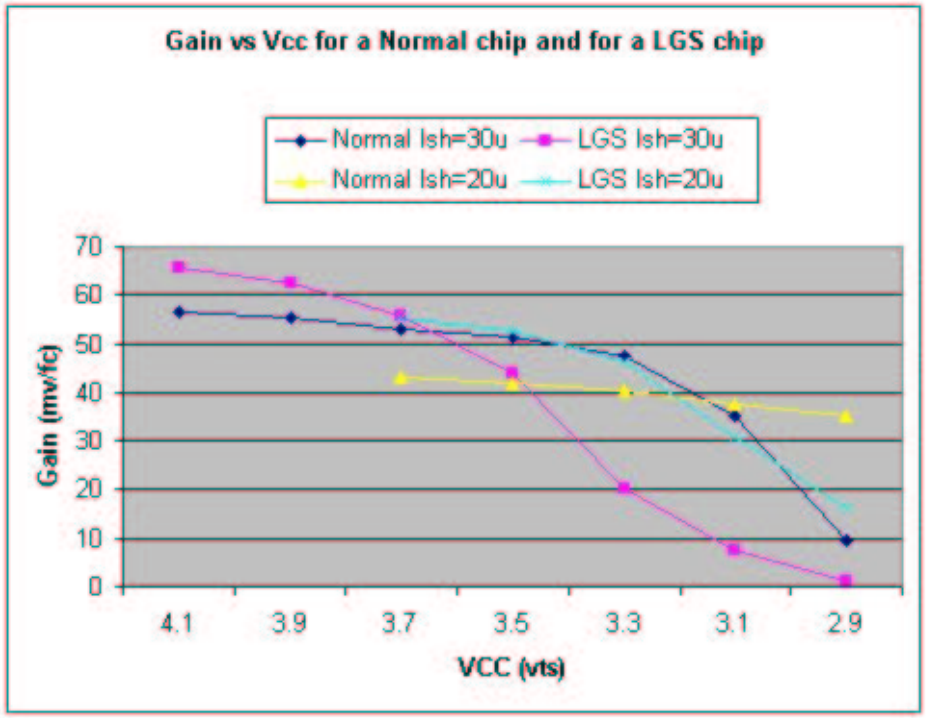
For the chip with LGS the gain is regular starting at Vcc=3.6V

or at Vcc=3.5V (nominal setting) and ISh=20 µA

Chip 0 of this hybrid is used here as a reference good chip

ISh/Vcc Study - Gain vs VCC and two ISh settings

Gain vs Vcc for Normal and LGS chips



From Bob Ely

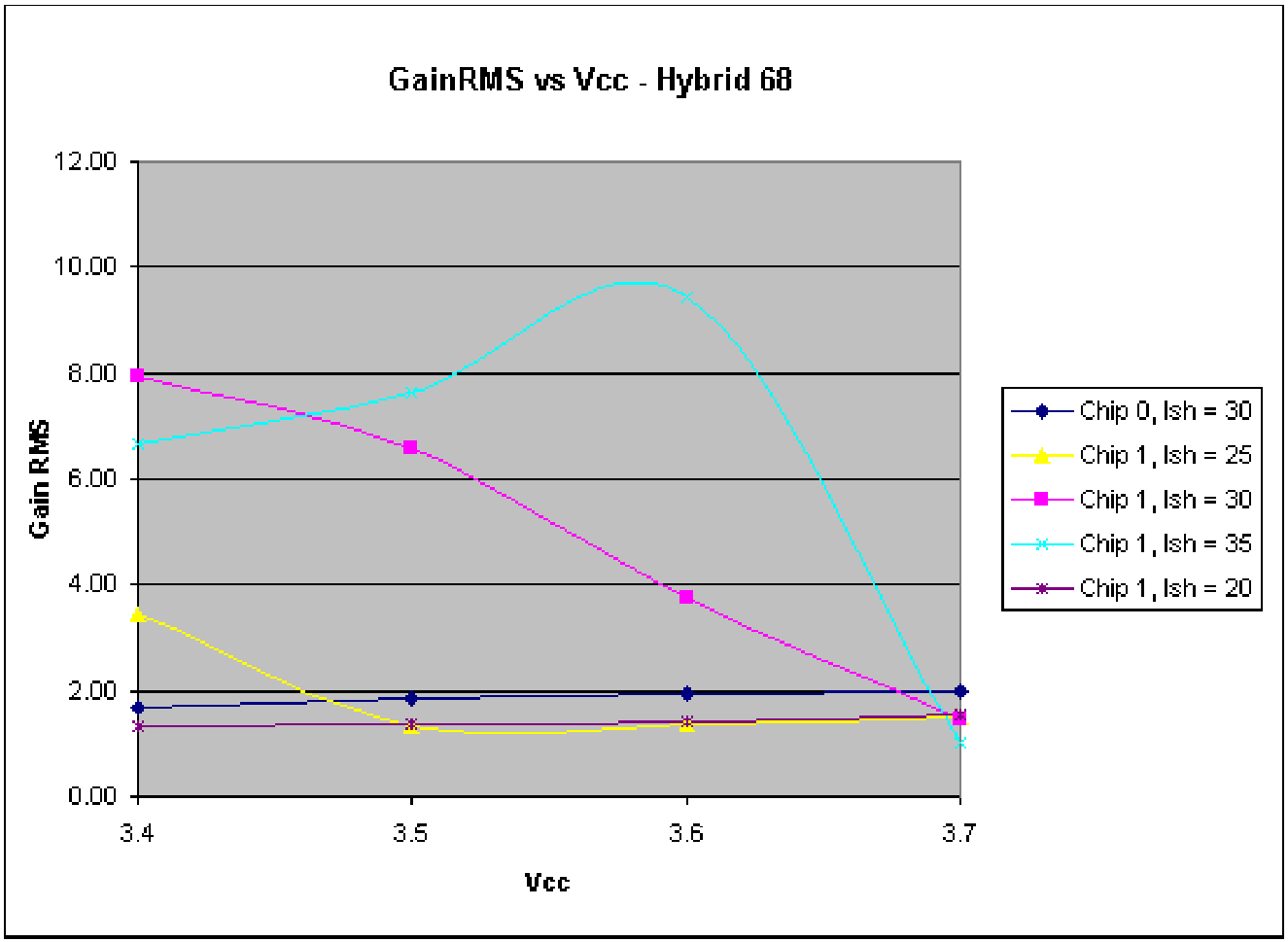
The gain vs Vcc characteristics for a normal chip and a LGS chip are clearly different when both are run with Ish =30µa.

The gain vs Vcc for the LGS chip with Ish = 20µa is very similar to the curve for the normal chip when Ish = 30µa.

The Ish current mirror is used 6 times in each channel and 6*128*10µa = 7.68ma which is about the excess current observed in the ICC plot.

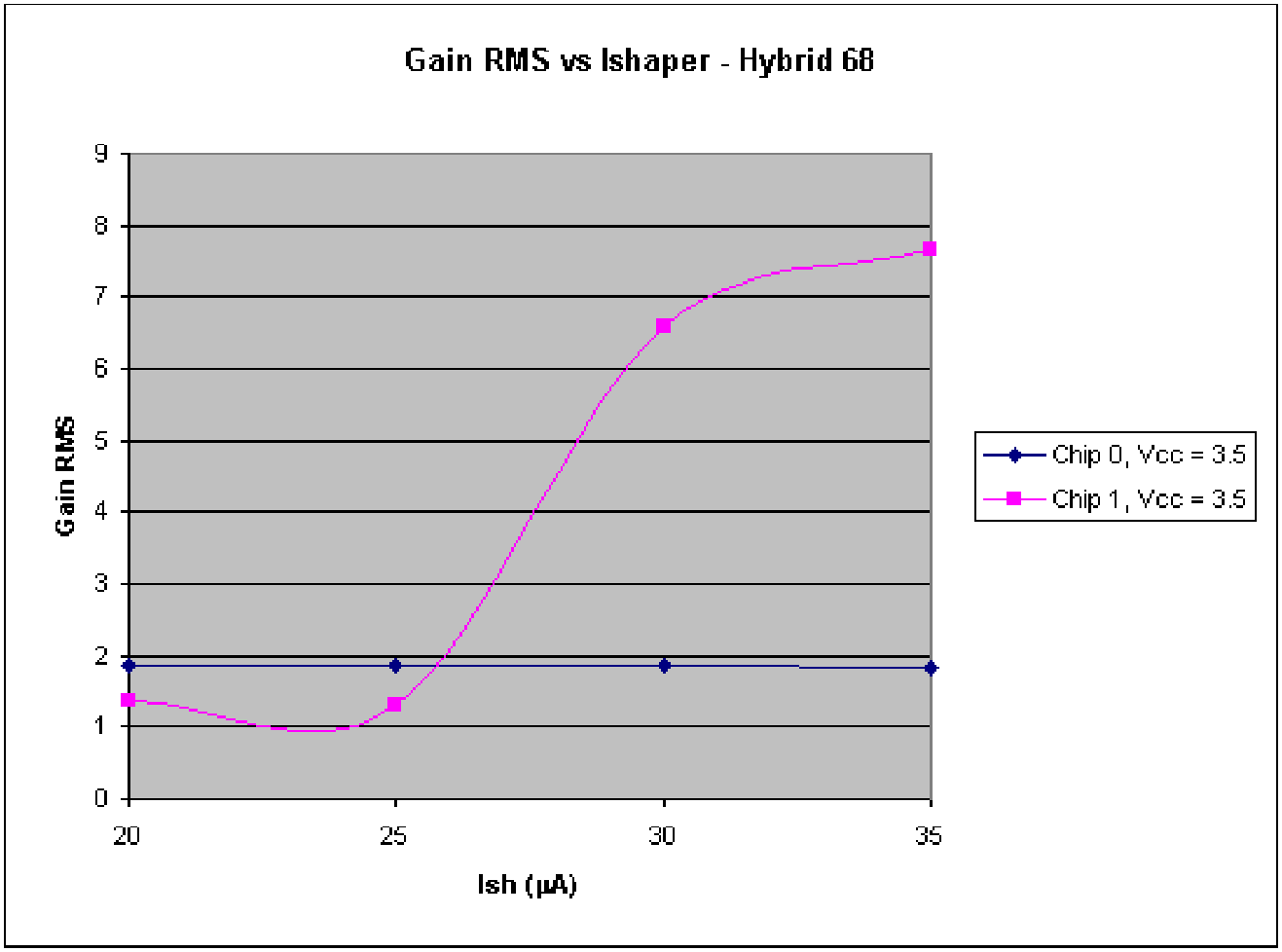
Is the shaper current abnormally large in the LGS chips and if so, is this the only difference?

Ish/Vcc Study - Gain RMS vs Vcc and several ISh settings



Chip 0 is used here as a reference good chip

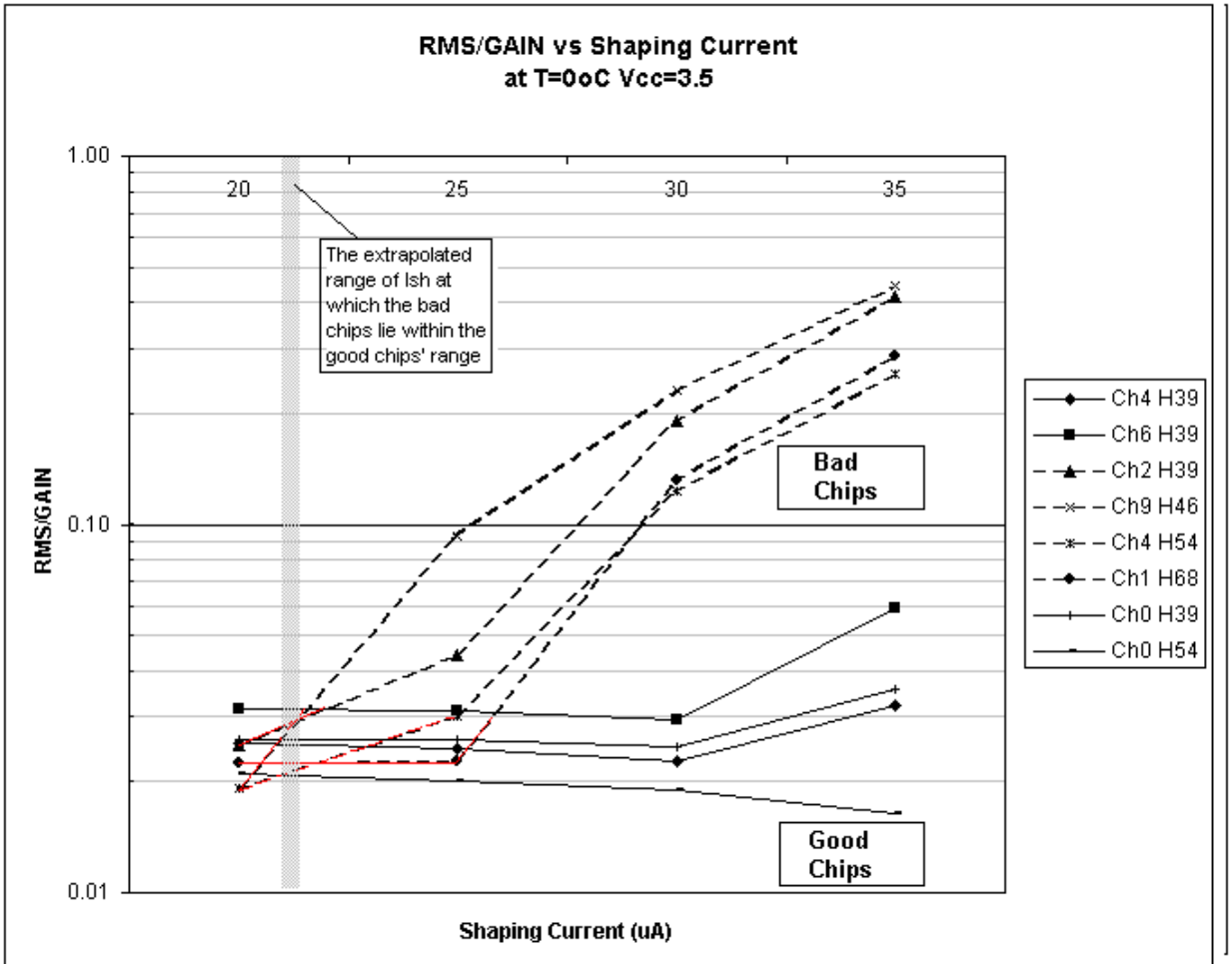
Ish/Vcc Study - Gain RMS vs ISh



Vcc=3.5V (nominal)

Chip 0 is used here as a reference good chip

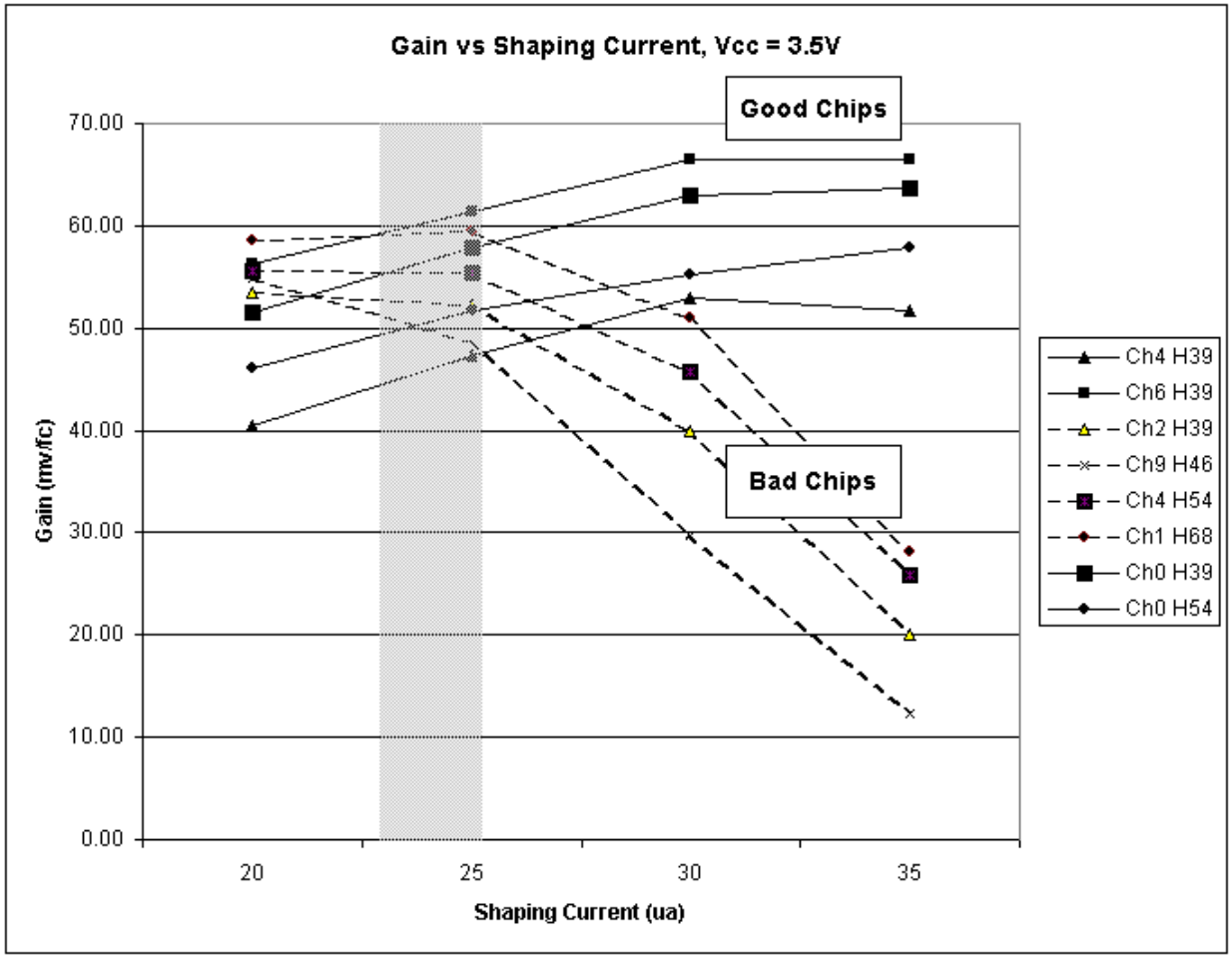
Ish/Vcc Study - Comparison for all Hybrids
Gain RMS vs ISh



There is a small range of Shaper Current (between 20μA and 22.5μA) where the defective chips have an extrapolated Gain Spread that lies within the range spanned by the tested good chips.

NOTE: the RMS/ Gain scale is plotted on a logarithmic scale, to better view the overlapping region.

Ish/Vcc Study - Comparison for all Hybrids
Gain vs ISh



As a trend, in this data range, increasing the Shaping Current increases the Gain of the passable chips and decreases the gain of the LGS chips.

In a range between 22.5μA and 25μA, the gain of the LGS chips is within an acceptable range

Icc Study

We looked at Icc (at the wafer level) for all the chips used so far in the US to verify a possible correlation with the LGS problem.

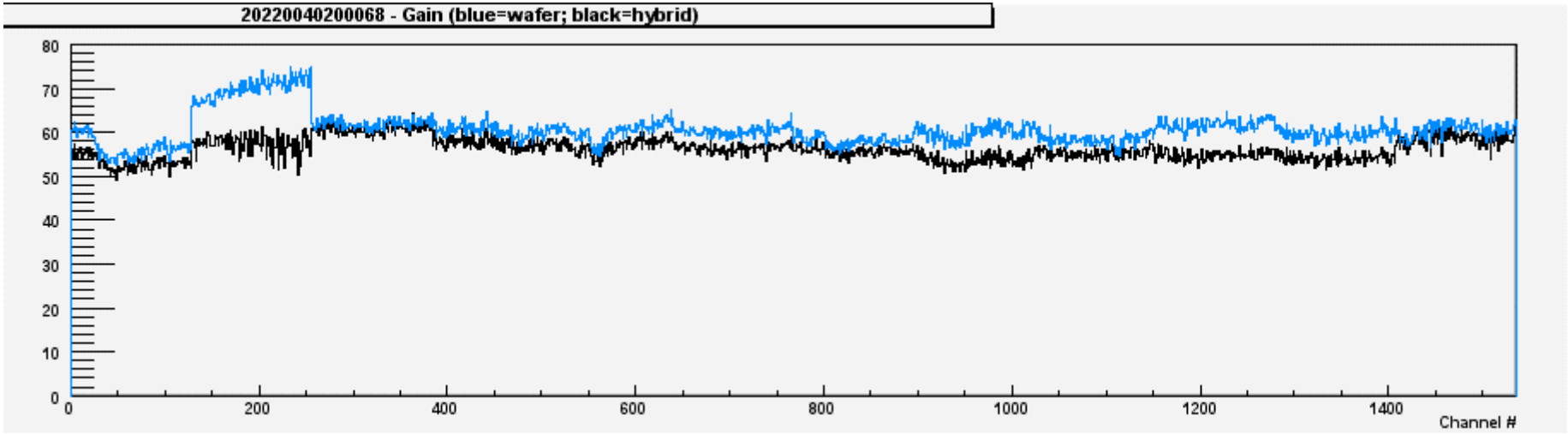
Having found that chips with LGS start to work normally mainly by lowering their Shaper current, and knowing that those chips have a strong dependence on the FE current, we are very likely facing a real defect for those chips in the distribution and regulation of the FE power that might cause an excessive current in the FE.

We found indeed a very strong correlation between high Icc and chips with LGS.

All our chips with LGS have much higher Icc (on the wafer).

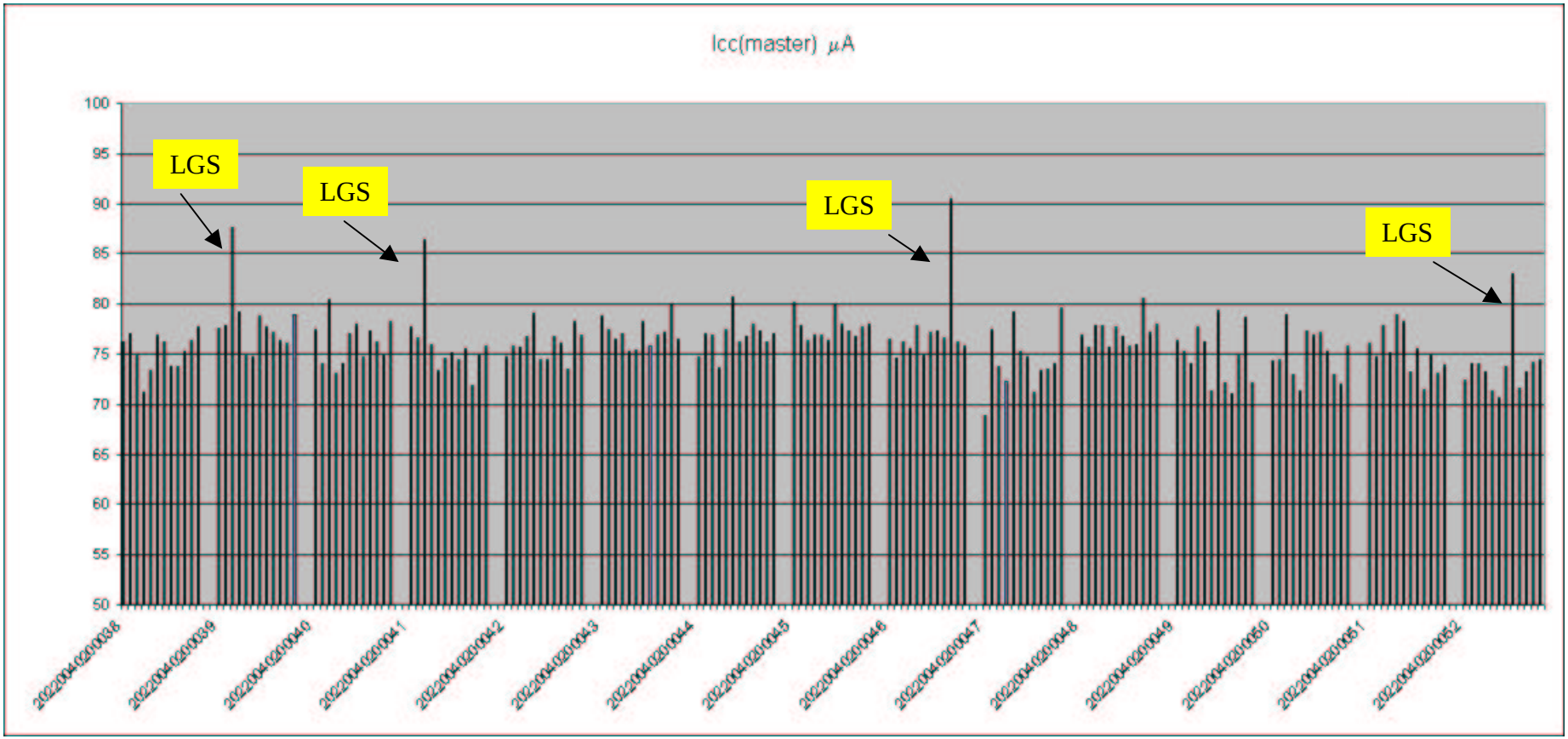
http://www-atlas.lbl.gov/strips/modules/production/lgs-study/Icc/

Icc Study – Wafer/Hybrid Comparison



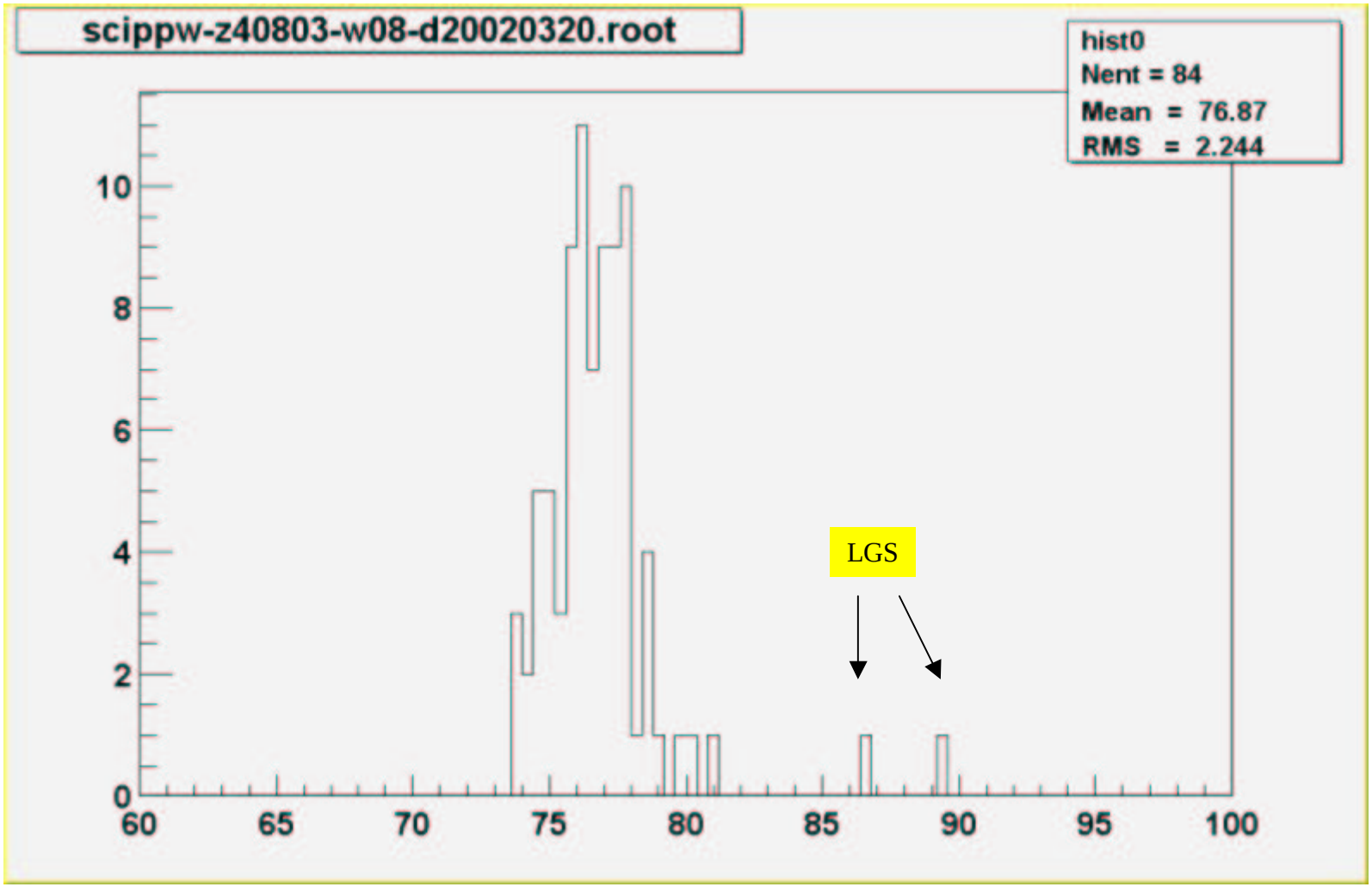
Icc Study – High Icc

Graph showing Icc of 15 hybrid. Chips that are known to have LGS show higher Icc
Similar graphs were produced for the 107 hybrids analyzed (1284 chips total)
17 chips were found having LGS (and higher Icc)



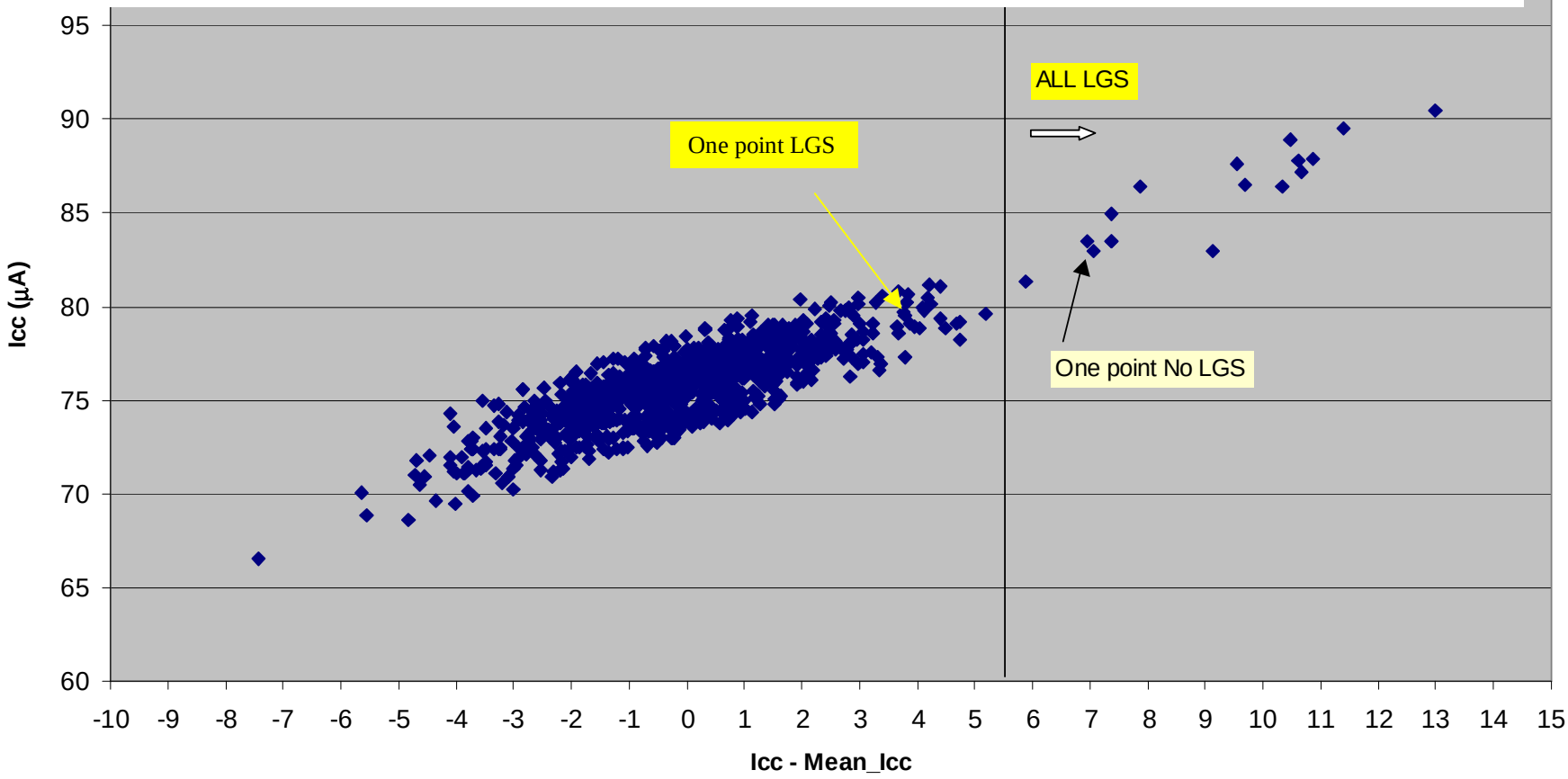
Icc Study – Icc distribution

A typical distribution of Icc per wafer showing large deviation for LGS chips



Icc Study – Icc vs (Icc-mean) Correlation

Scatter plot of Icc versus the deviation of Icc from the mean Icc for each wafer (or gelpak) each chip is coming from All but one of the 17 chips with LGS can be identified by cutting at 5.5 (deviation from the mean Icc). This method can be used for pre-selecting chips before they are mounted on hybrids



DAC Study

A possible explanation for the tail in the Icc distribution can be that the actual values of bias currents set by DACs (the shaper one in particular) are higher than the nominal one.

This would also agree with her observation that lowering the value of the shaper DAC brings the shaper closer to the normal operating value.

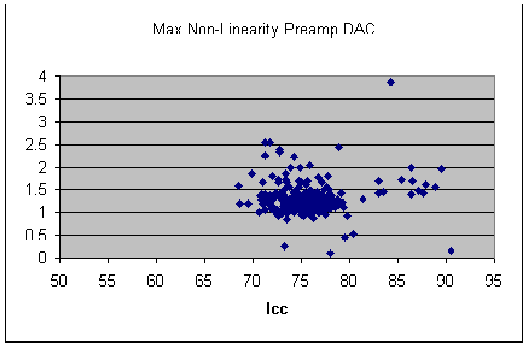
The values of the DACs non-linearity, slope and offset are taken from
the results of the wafer test data

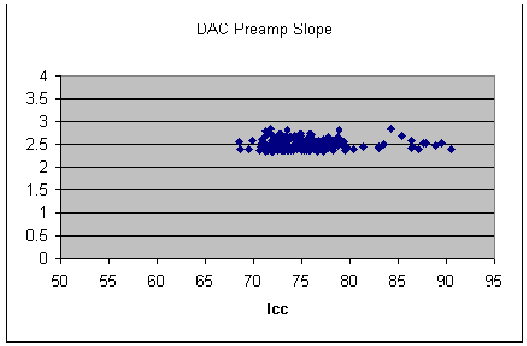
Z41032	W13 chip# 15 and 140		
Z40802	W09 chip# 30		
Z40859	W03 chip# 247	W04 chip# 223	
Z40803	W02 chip# 132	W05 chip# 18 and 158	W08 chip# 25 and 111
Z40862	W02 chip# 232	W09 chip# 102 and 215	

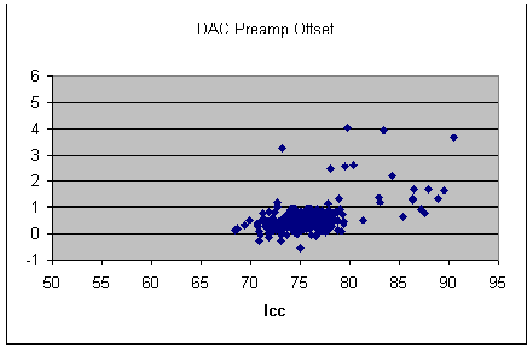
http://www-atlas.lbl.gov/strips/modules/production/lgs-study/DAC/

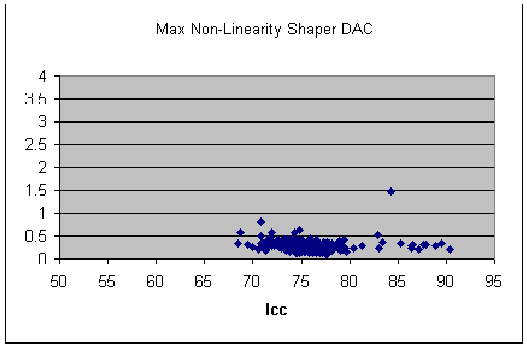
DAC Study – all DATA

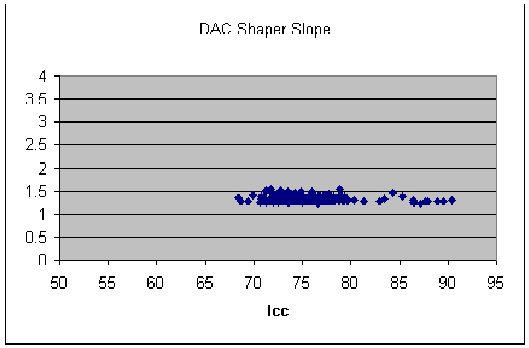
A strong correlation between LGS chips and Shaper DAC offset is found from this study

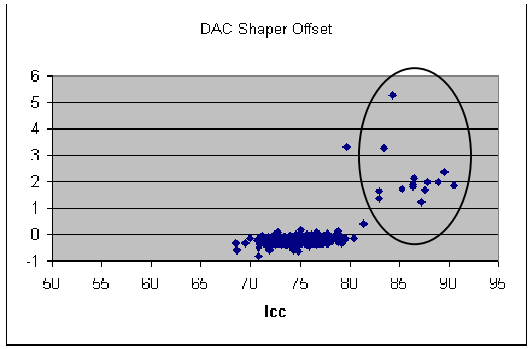




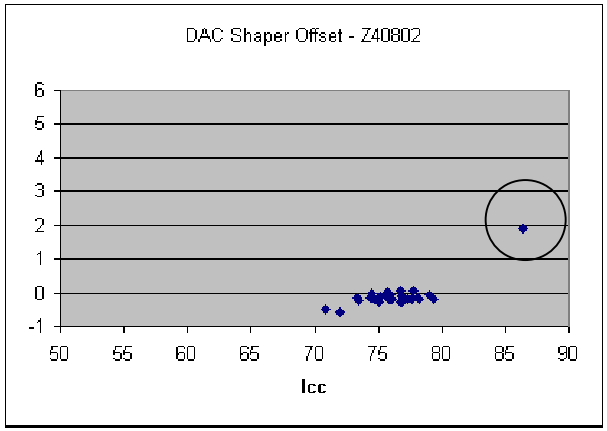


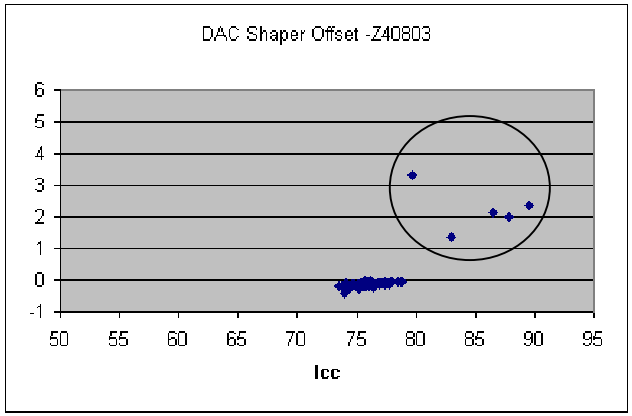


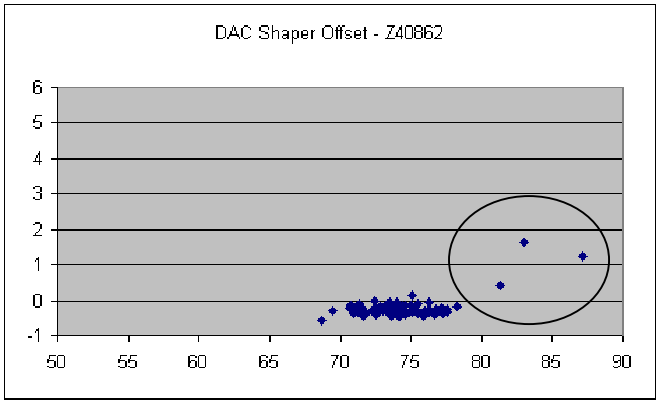


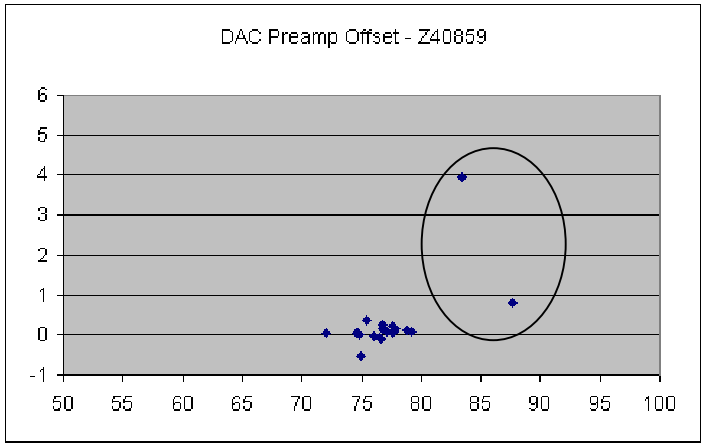


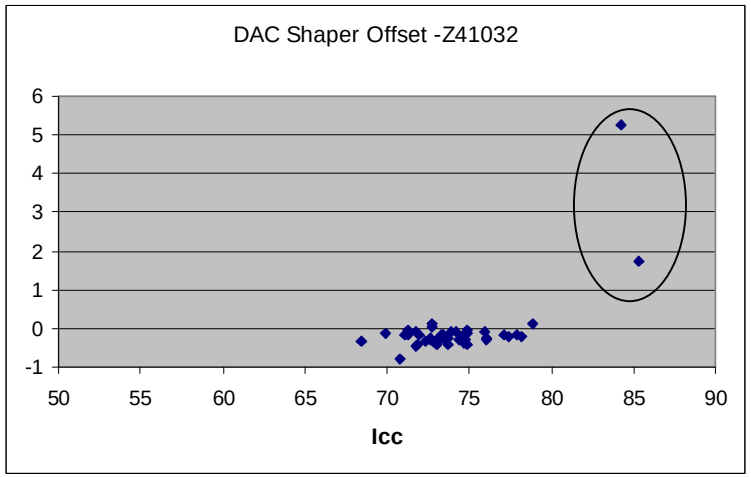
DAC Study – Shaper DAC offset











DAC Study – Shaper DAC Fit

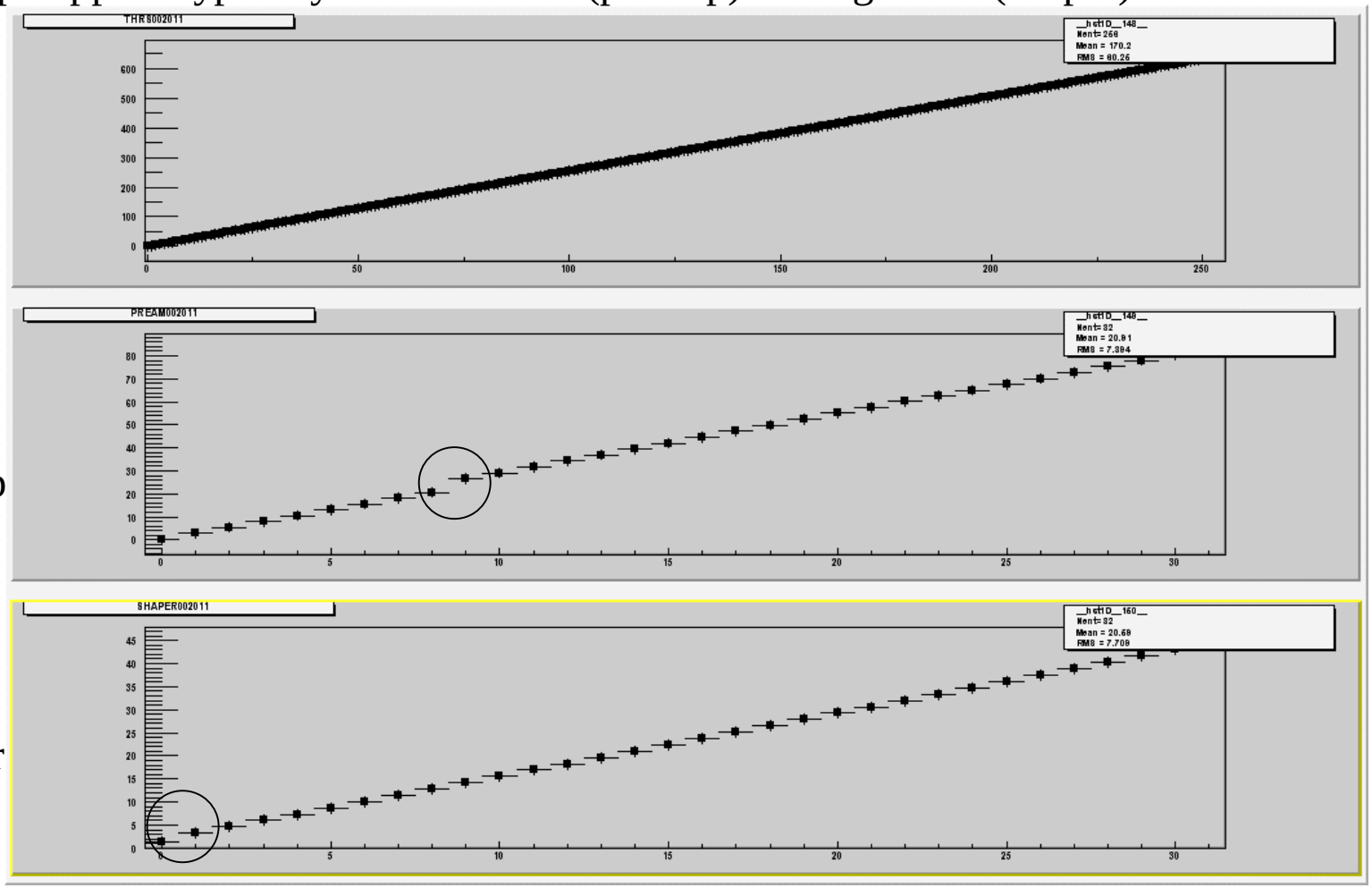
Z41032-W13-#140

A jump happens typically between 5-10 (preamp) and right at 1 (shaper)

thr

preamp

shaper



DAC Study – Shaper DAC Fit

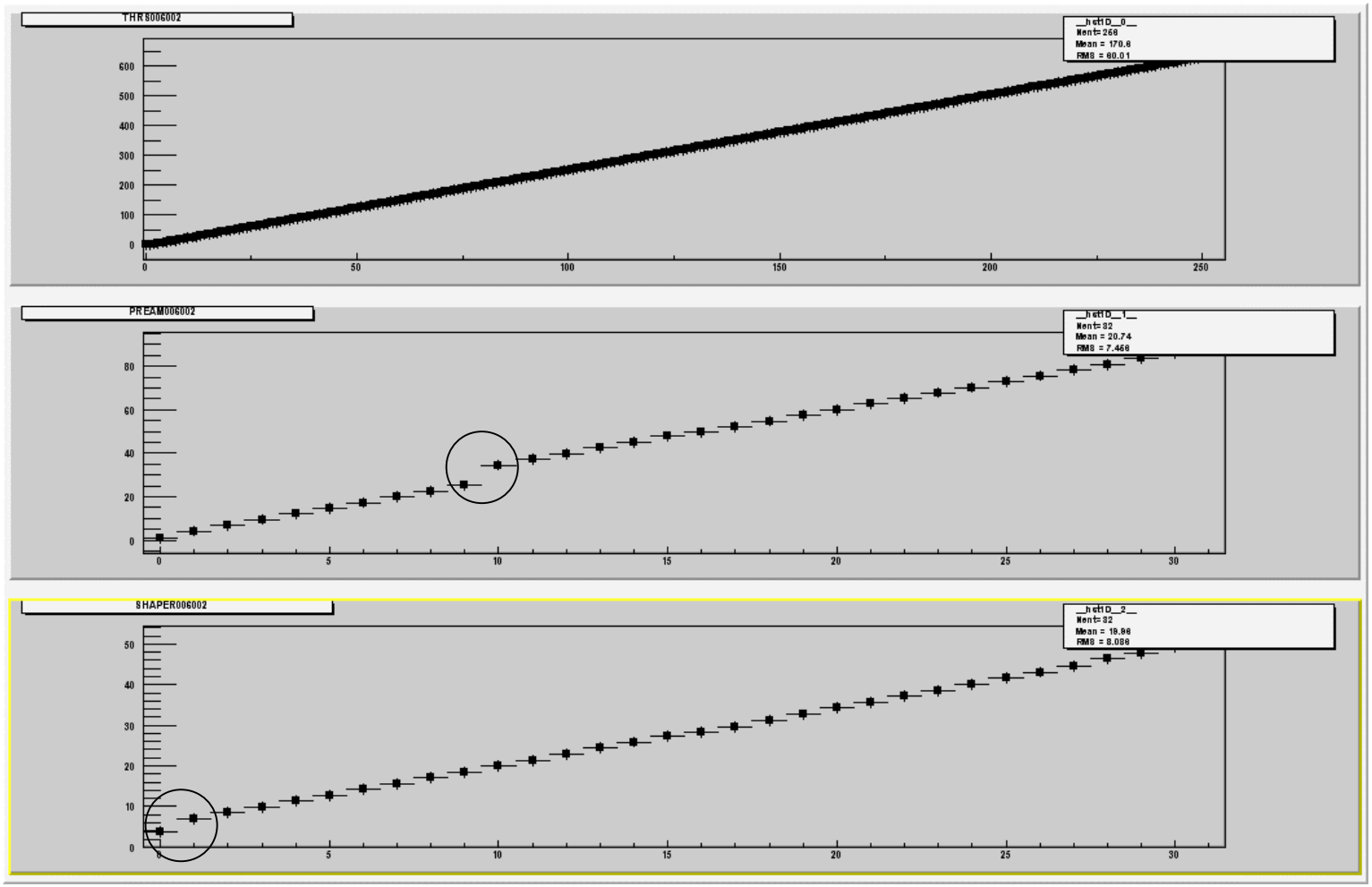
Z41032-W13-#15

A jump happens typically between 5-10 (preamp) and right at 1 (shaper)

thr

preamp

shaper



DAC Study – Shaper DAC Fit

Z41032-W13-#26

Good chip

thr

preamp

shaper