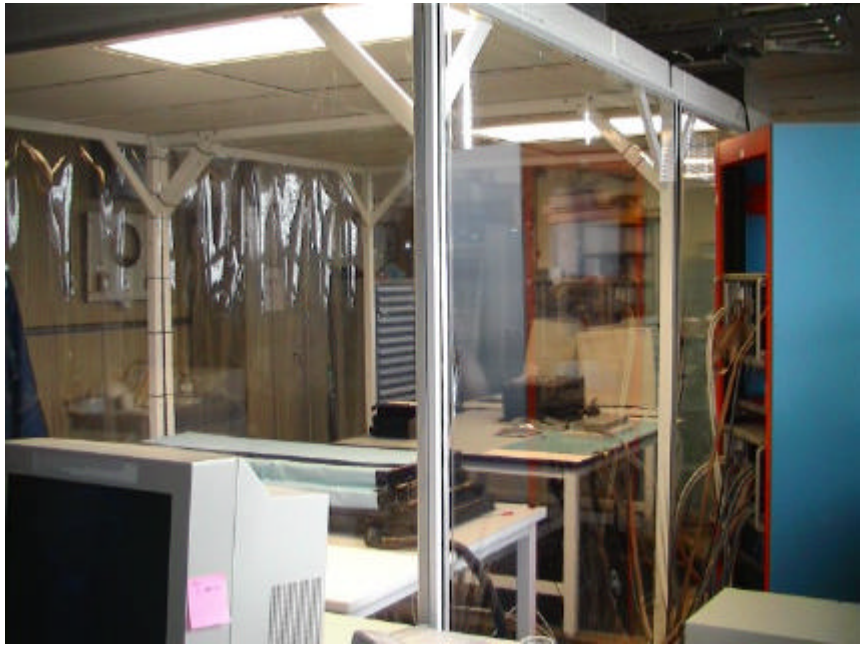
US Hybrid/Module Production Test Results

- Status
  - Wafer used
  - Chip status
  - Channel Summary
- Overall Issues
  - Chip QA
  - Chip Replacement
  - Wafer/Hybrid Comparison
  - Gain (non) uniformity
  - Wafer/Hybrid Correlation
  - Gain Spread at cold
  - Testing Time
- *Modules*



Status

29 Hybrids

- Built
- Burn-in at 37^{o}C
- LTT at 0^{o}C
- 12 ready to module

3 Modules built and partially tested

8+(16) new Hybrids under assembly

Wafers Used

Distribution of chips on hybrid by Wafer

Z40859-W11	Z40859-W14
20220040200008: Chips 00-11 20220040200009: Chips 00-11 20220040200011: Chips 00-11 (Chip 11 replaced)	20220040200023: Chips 00-11 20220040200024: Chips 00-11 20220040200025: Chips 00-11 20220040200020: Chips 00-11 (Chip 01 replaced)
Z40800-W13	**Z40859-W03**
20220040200010: Chips 00-11 20220040200012: Chips 00-11	20220040200026: Chips 00-11 20220040200028: Chips 00-11 20220040200030: Chips 00-11 20220040200031: Chips 00-11 20220040200036: Chips 00-06, 08-11
Z40859-W02	**Z40859-W01**
20220040200013: Chips 00-11 20220040200014: Chips 00-11 20220040200015: Chips 00-11 20220040200016: Chips 00-11 20220040200017: Chips 00-11 20220040200033: Chip 00 20220040200034: Chip 01 20220040200035: Chip 09 20220040200036: Chip 07 20220040200020: Chip 01 (replacement)	20220040200027: Chips 00-11 20220040200029: Chips 00-11 20220040200033: Chips 01-11 20220040200035: Chips 00-08, 10-11
Z40859-W09	**Z40859-W04**
20220040200018: Chips 00-11 20220040200019: Chips 00-11 20220040200021: Chips 00-11 20220040200022: Chips 00-11	20220040200032: Chips 00-11 20220040200034: Chips 00, 02-11 20220040200037: Chips 00-11

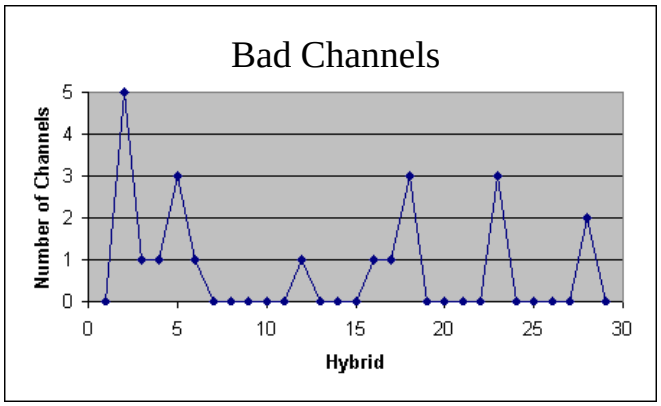
Chip Status

20220040200011	Chip 11	replaced	Large Gain Spread
20220040200013	Chips 2-5	---	All Digital tests failure at 33°C
20220040200020	Chip 1	replaced	TOKEN failure
20220040200021	Chip 8	---	Large Gain Spread
20220040200022	Chip 10	---	High Offset
20220040200035	Chip 6 (M8)	---	Time Walk test failure

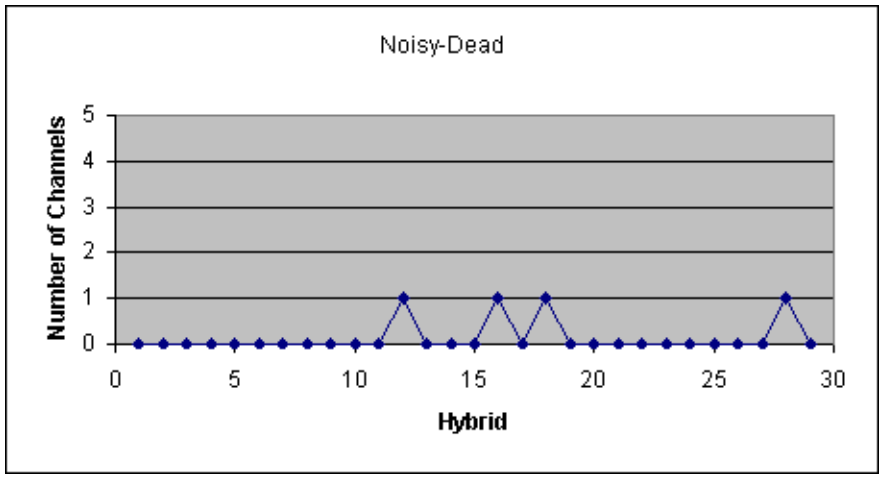
+1 chip chipped and replaced right away

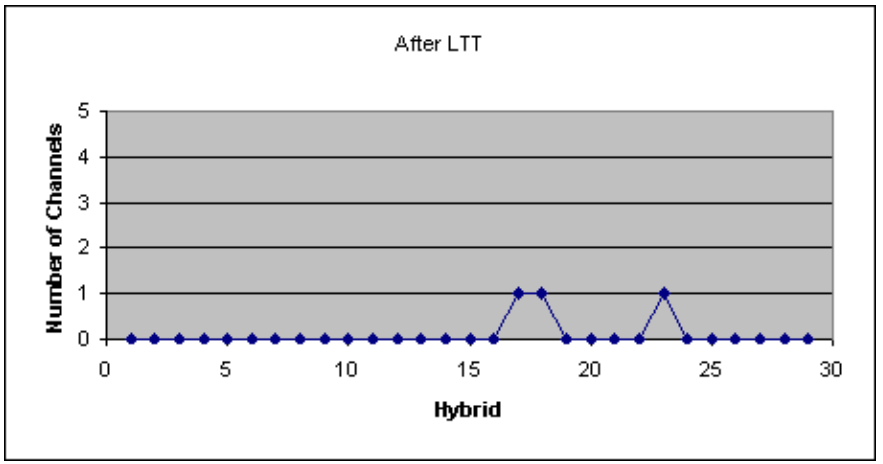
Hybrid Bad Channel Summary

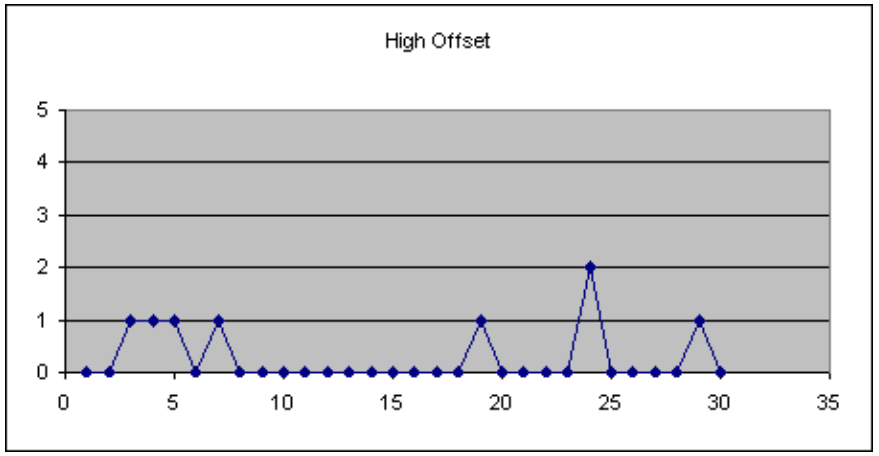
Serial #	Dead/ defect	partbonded (high noise)	NoisyHead	After LTT	High Offset (>50)	#lost after fanout	Total bad channels (hybrid)
20220040200008	0	0	0	0	0	0	0
20220040200009	0	0	0	0	1	4	5
20220040200010	0	0	0	0	1	0	1
20220040200011	0	0	0	0	1	0	1
20220040200012	0	0	0	0	0	3	3
20220040200013	0	0	0	0	1	0	1
20220040200014	0	1	0	0	0	0	0
20220040200015	0	10	0	0	0	0	0
20220040200016	0	0	0	0	0	0	0
20220040200017	0	10	0	0	0	0	0
20220040200018	0	0	0	0	0	2	2
20220040200019	0	0	1	0	0	0	1
20220040200020	128	0	0	0	0	0	0
20220040200021	0	9	0	0	0	0	0
20220040200022	118	28	0	0	0	0	0
20220040202223	0	0	1	0	0	0	1
20220040200024	0	1	0	1	0	0	1
20220040200025	0	0	1	1	1	0	3
20220040200026	0	0	0	0	0	0	0
20220040200027	0	0	0	0	0	0	0
20220040200028	0	0	0	0	0	0	0
20220040200029	0	60	0	0	0	0	0
20220040200030	0	0	0	1	2	0	3
20220040200031	0	0	0	0	0	0	0
20220040200032	0	0	0	0	0	0	0
20220040200033	0	0	0	0	0	0	0
20220040200034	0	2	0	0	0	0	0
20220040200035	0	0	1	0	1	0	2
20220040200036	0	0	0	0	0	0	0

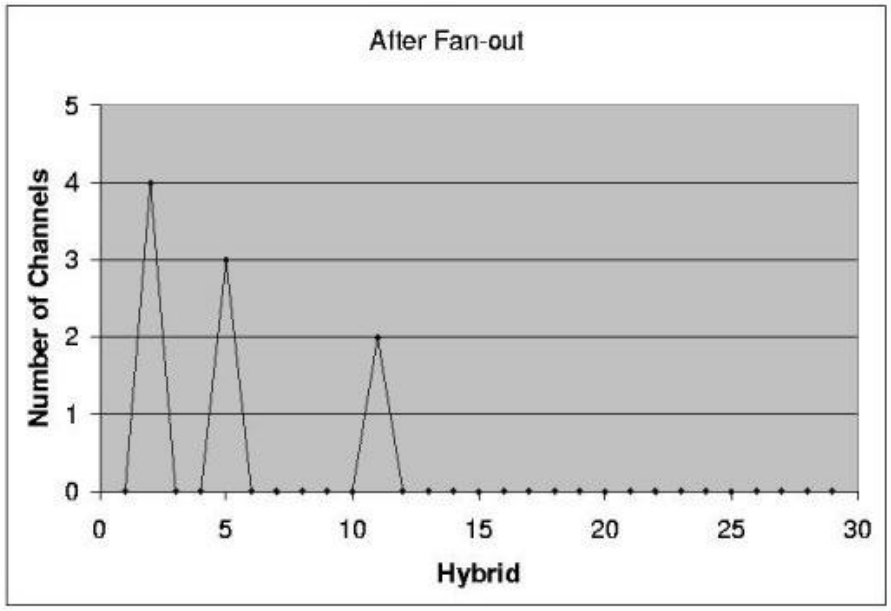


Bad Channels (detailed)









Overall Issues

- Chip QA
  - Visual inspection
  - Wafer/Hybrid Comparison used to decide when a chip needs to be replaced

- Gain non-uniformity (but mostly in agreement with wafer data)
  - Wafer/Hybrid Comparison to confirm chips are within spec → *See W/H Correlation Study*
  - Possible chip pre-selection/better matching from looking at Wafer data of chips available to use

- Gain higher and oscillating for several chips on a given hybrid at 0^{o}C (Hybrid LTT) after trim
  - The threshold DAC has a tendency to saturate.
  - This effect kicks in at slightly lower thresholds as a hybrid is cooled down.
  - The 8fC point is out of line (off to higher threshold) during low temperature tests.
  - For some hybrids it can be seen also at room temperature.
  - This can effect the fitting of the response curve, hence the false high gain.
  - We might not include the 8fC point in the RC fit in the future.

- Testing Time – too long
  - LTT- Burn-in defects (no) time dependence

- Occasional channels with high offset which are manually masked to obtain a better NO curve
  - This effect could be reduced with new cuts

- Fan-out bonds pop-off for the first batch of hybrids and “hairy” bond foot
  - Unbonded channels will show up in modules but we know already of some through visual inspection
- New batch of hybrids with new metalization of the PA pads and no squeezed-out glue
  - Good results on mechanical hybrids

Chip QA

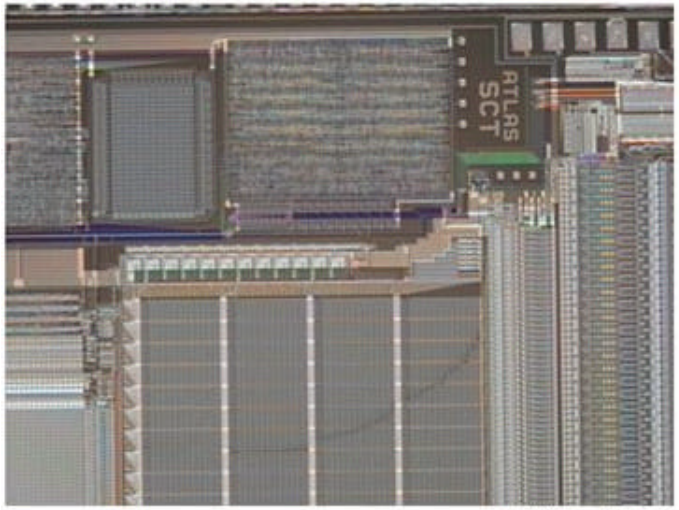
Visual inspection shows good quality of chips

- ~ 350 IC's used
  - 3 rejected (pictures)
  - 1 recovered

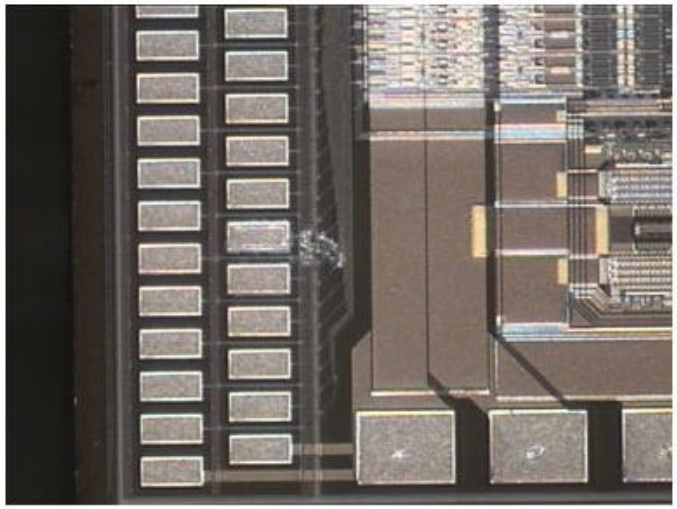
- 112 IC's being used
  - One rejected a few needed recovery (pictures)

Chip QA Pictures

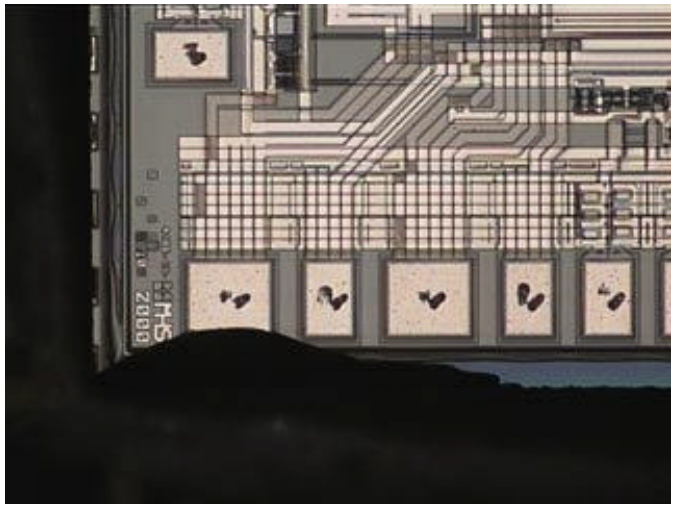
Chip 28 on Z40859-W03-1

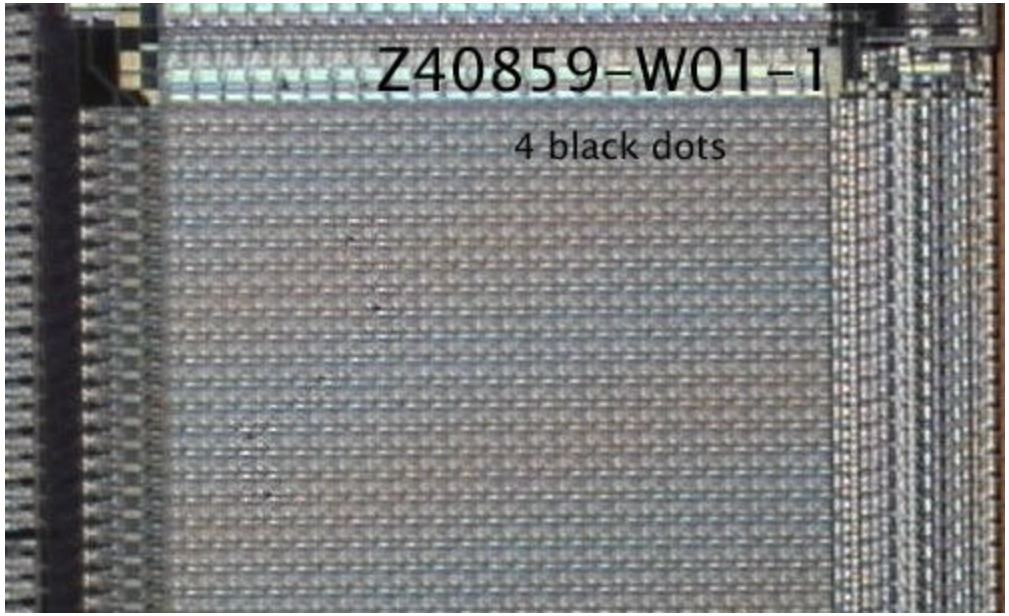


Chip 233 on Z40859-W09-2

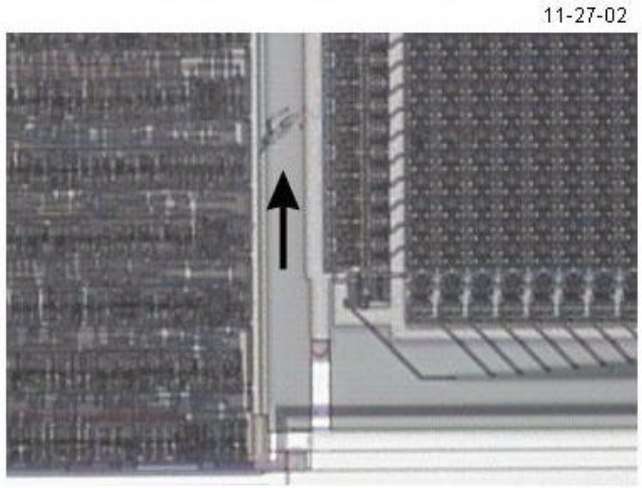


Z 40859-W02-1

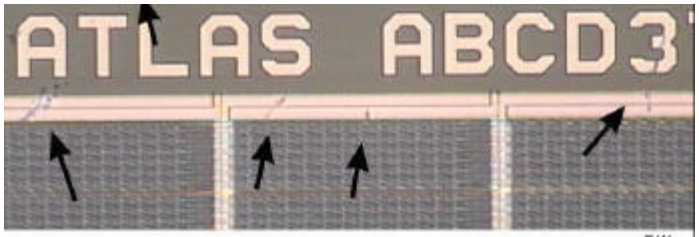




Chip QA Pictures (last batch)

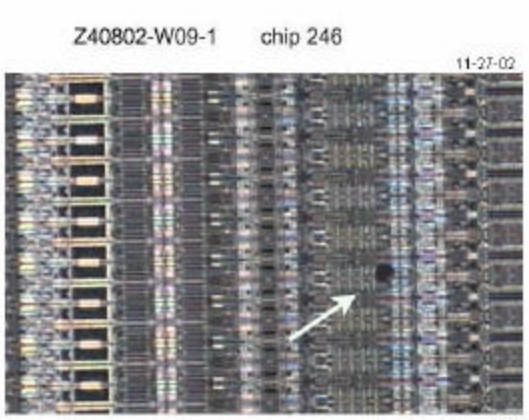


scratch

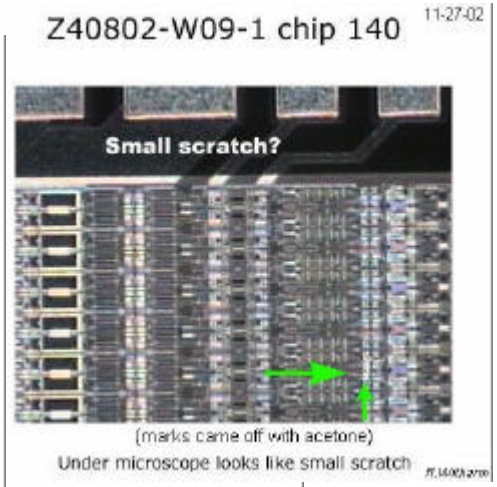


Scratches on surface

marks came off with acetone



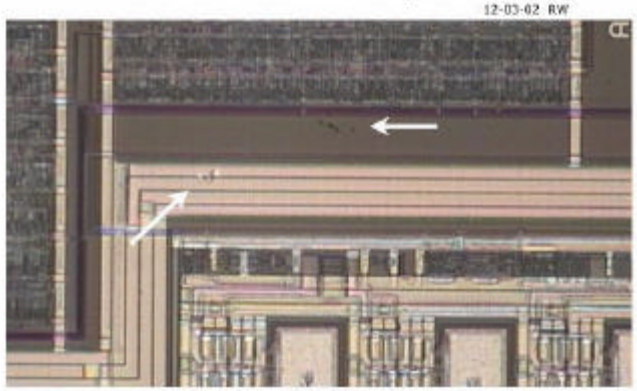
Chocolate colored spot on 2 chips
removed with acetone



(marks came off with acetone)
Under microscope looks like small scratch

chip 132

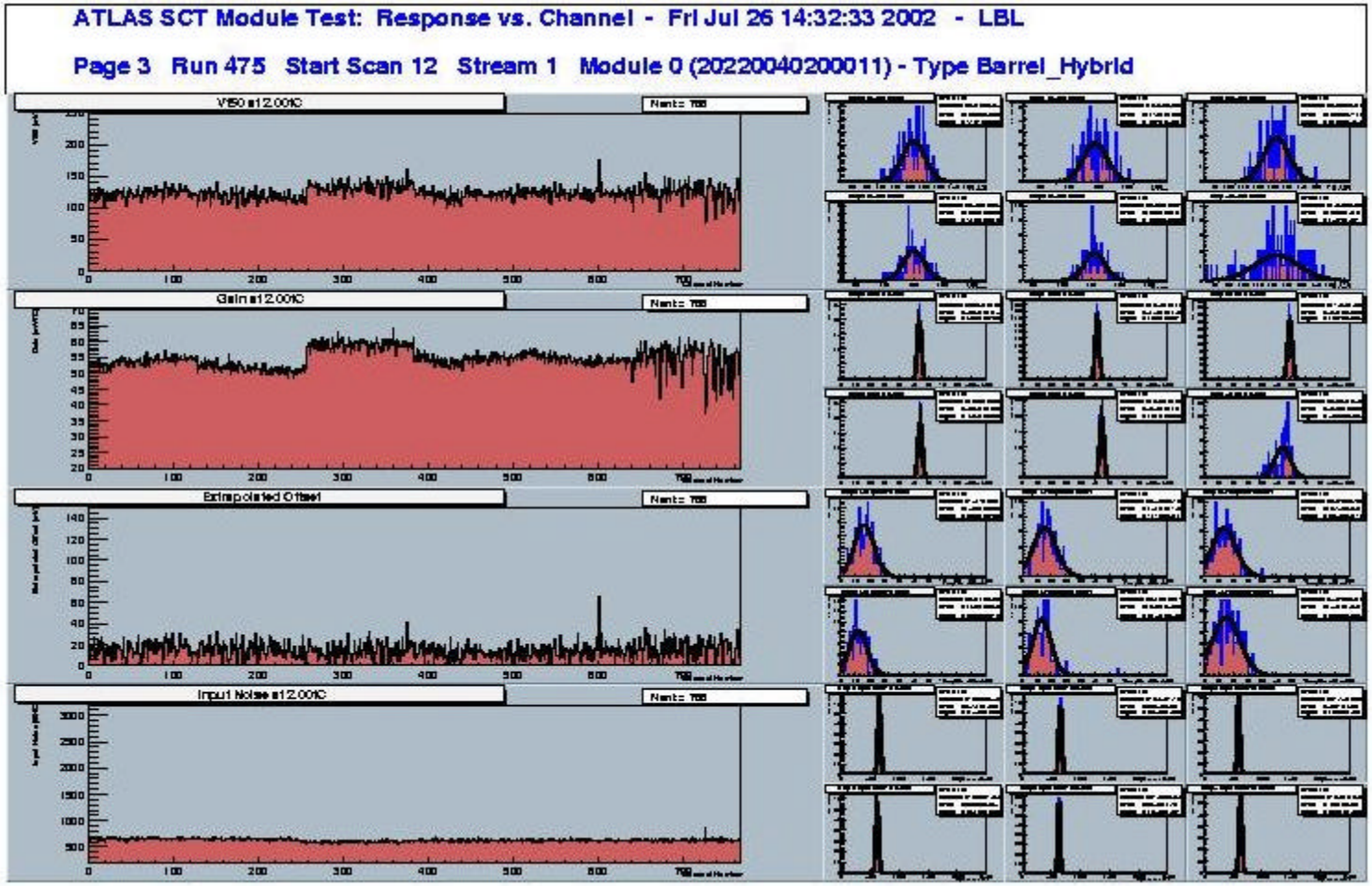
Z40802-W14-1 chip 19



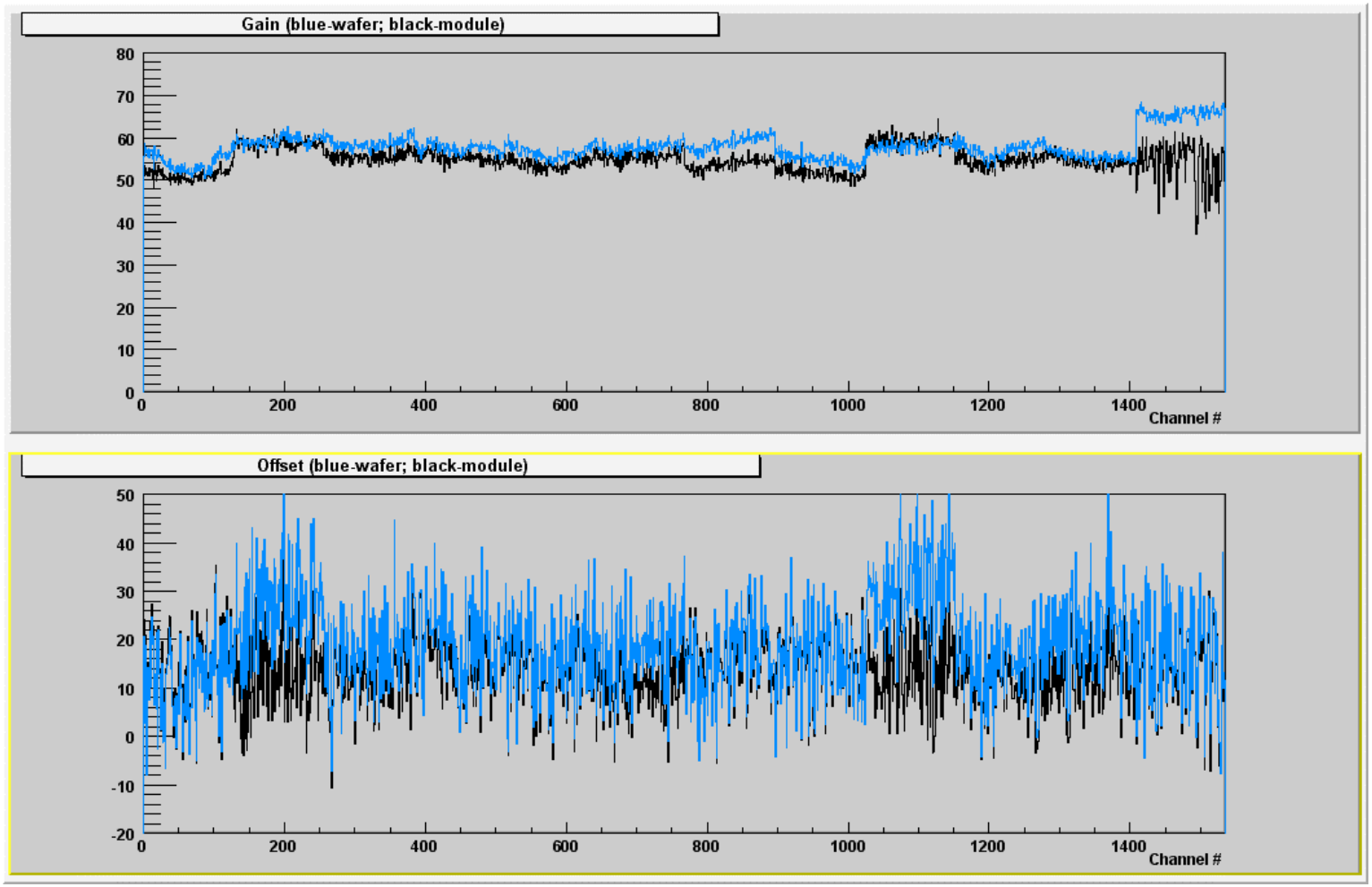
marks came off with acetone

Chip replacement 

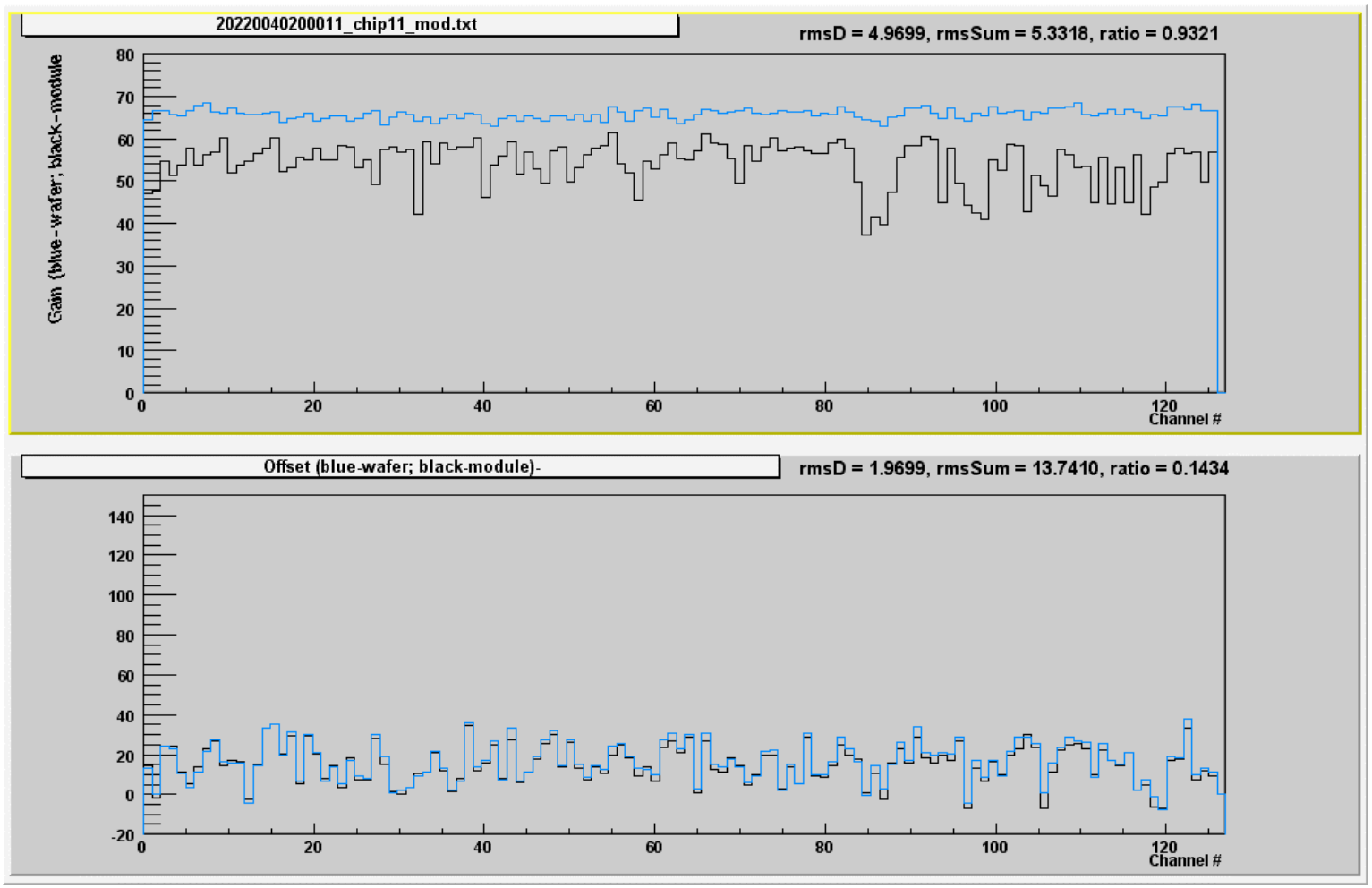
Hybrid 20220040200011
chip 11 Large Gain Spread



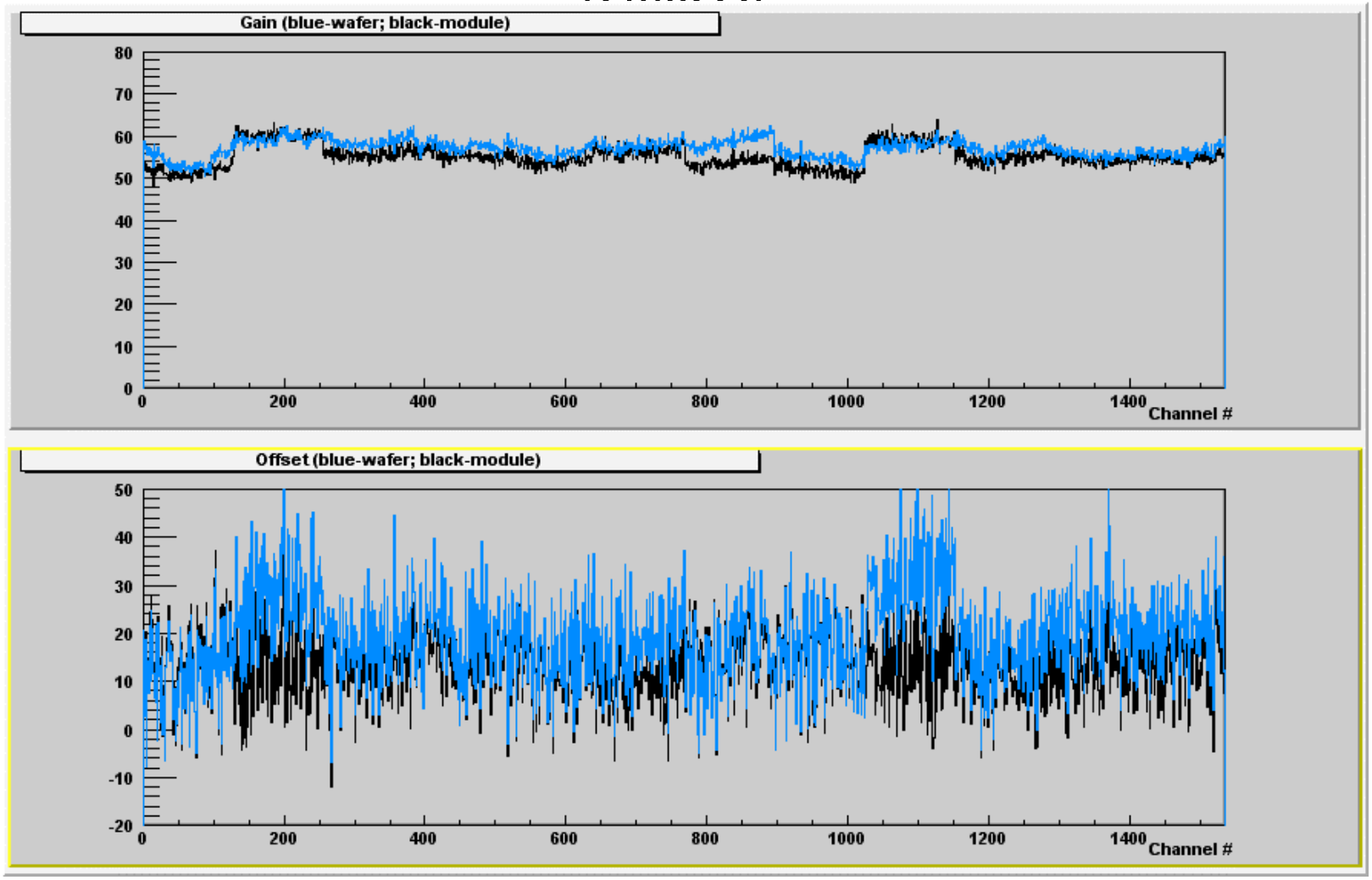
Hybrid 20220040200011
Wafer/Hybrid Comparison



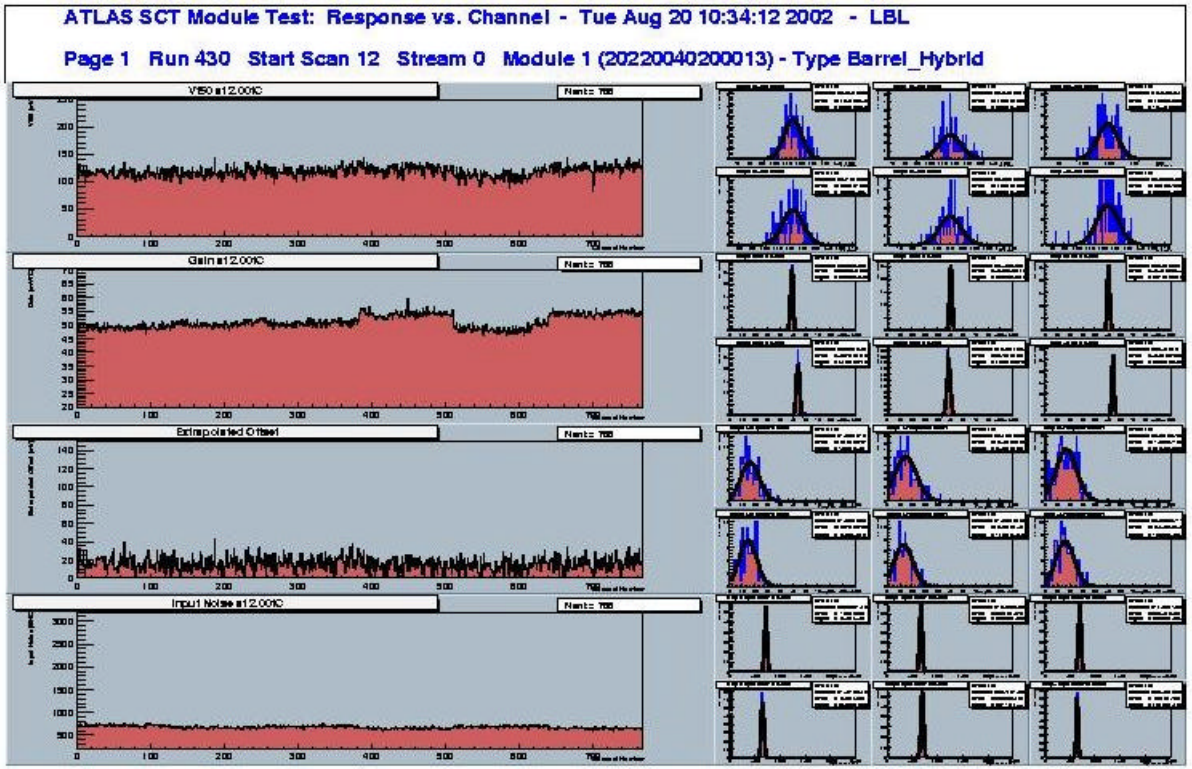
Hybrid 20220040200011
Chip 11 Wafer/Hybrid Comparison



Hybrid 20220040200011
Wafer/Hybrid Comparison after chip 11 replaced



Hybrid 20220040200013
Chip 2-5 Digital Tests Failure starting at 33°C



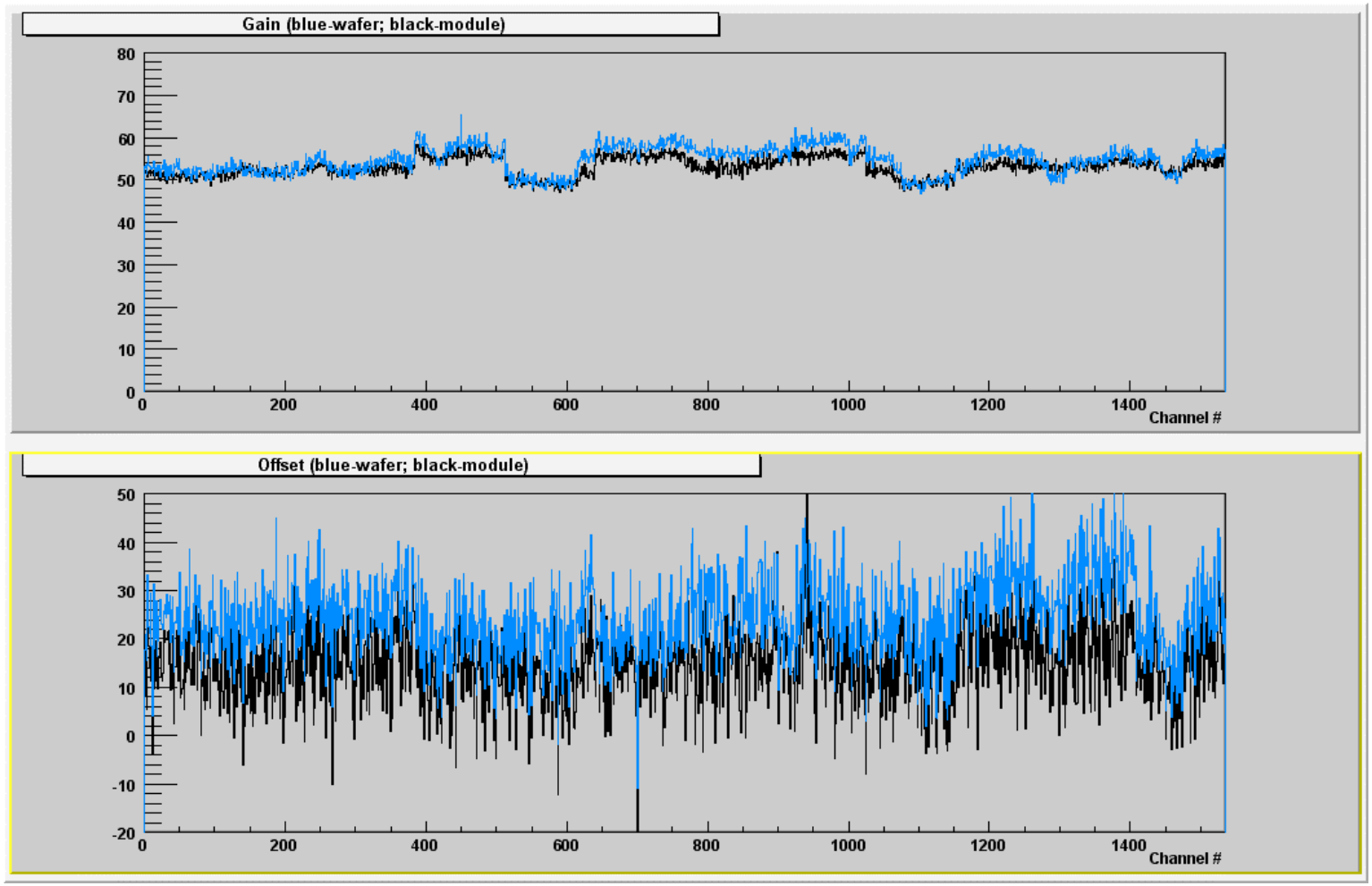
Three Point Gain Response at 37°C

Hybrid tests:
FullBypassTest: fails at Vdd = 3.5V but works fine at higher Vdd

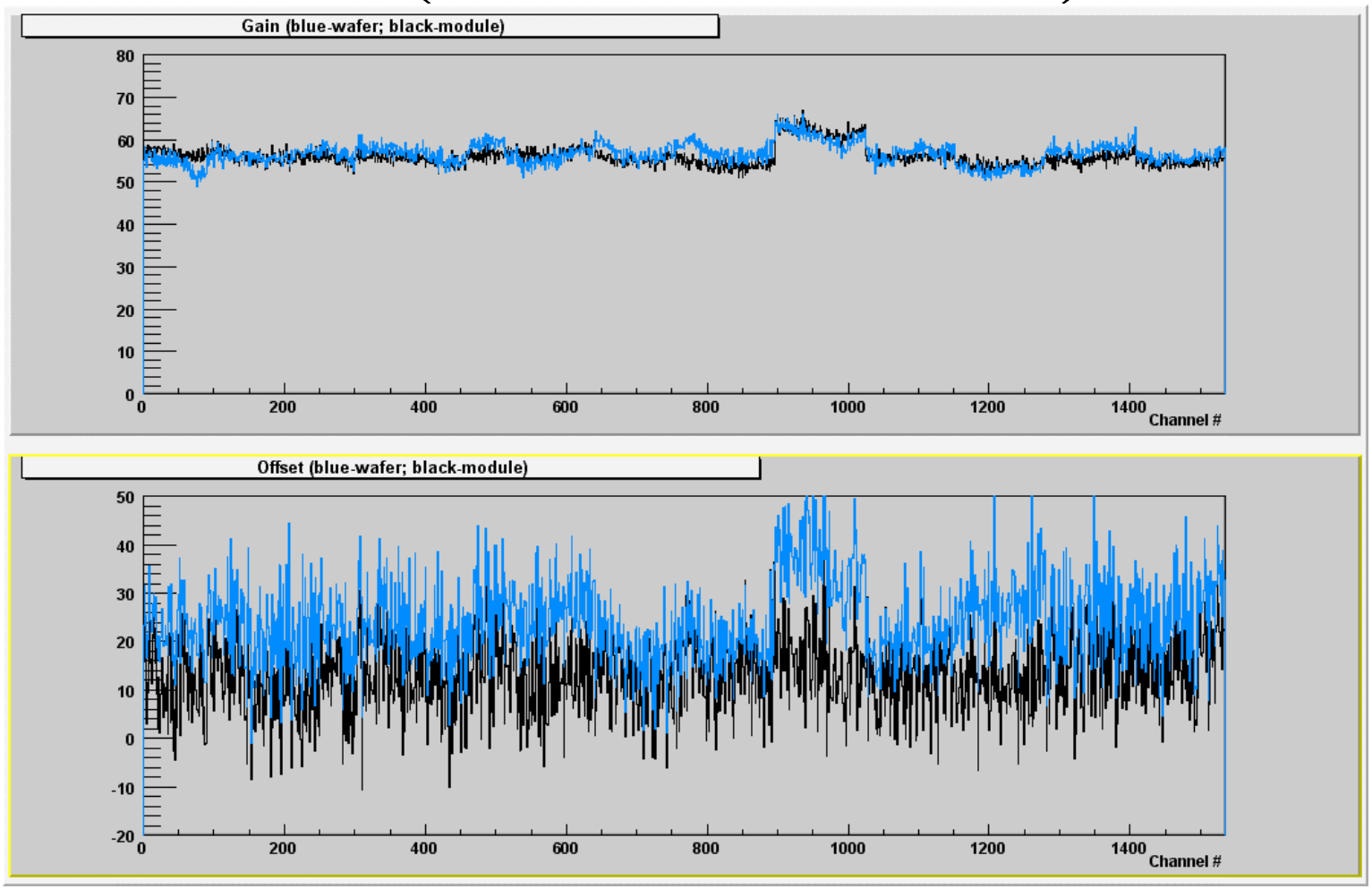
Wafer TV tests:
At 40 and 50 MHz all chips TV(eff) = 1 and all Vdd(eff) =1
except chip S02: at 50 MHz and Vdd=3.3V for TV2 to TV5 eff =0

The timing of the token passing is quite critical. At higher temperatures the CMOS is slower, so it could get closer to the edge.
It might be related to the quality of the clock signal.
It might work at a different system.

Hybrid 20220040200013
Wafer/Hybrid Comparison

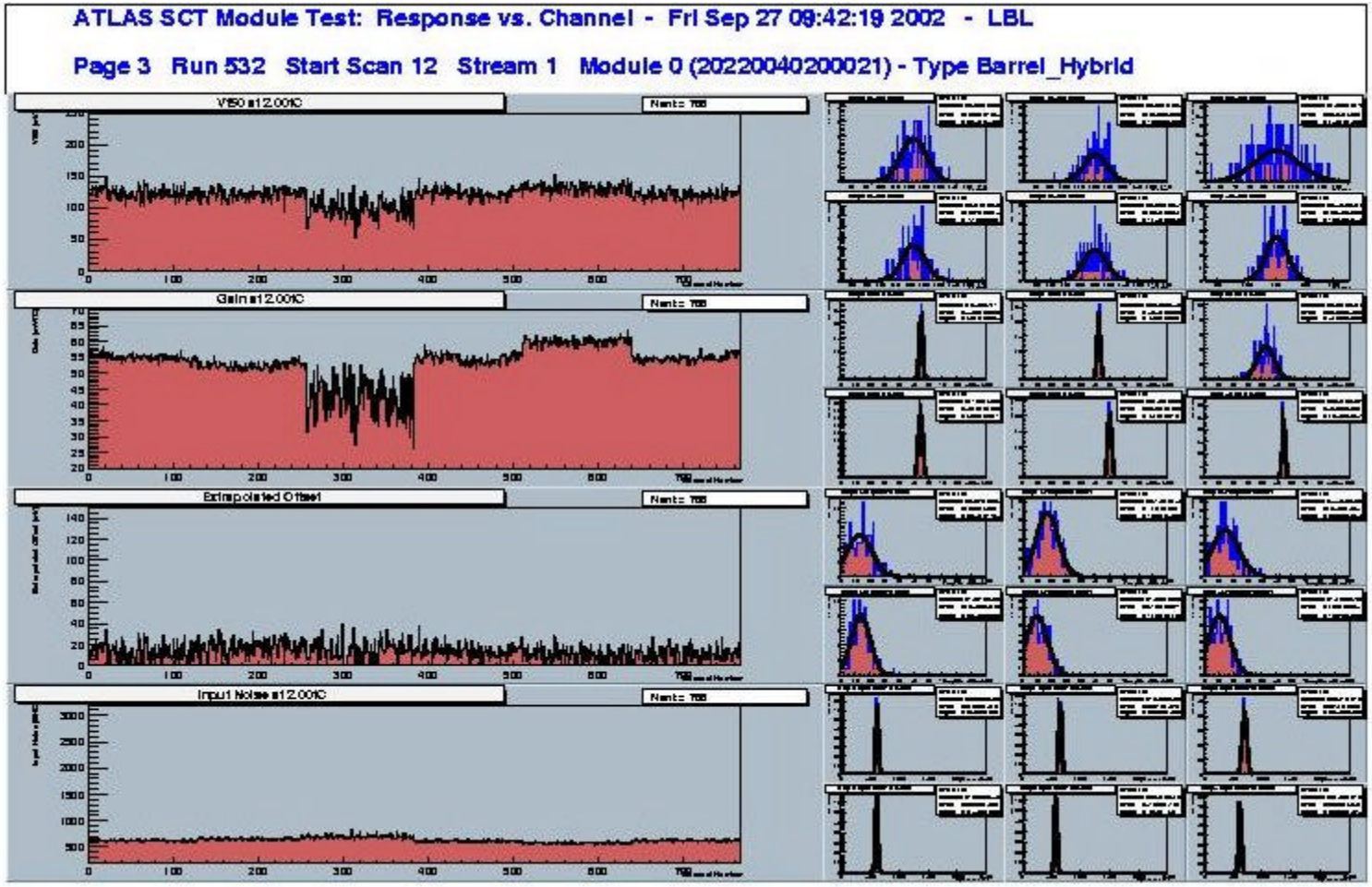


Hybrid 20220040200020
Wafer/Hybrid Comparison after chip 1 replaced (because of TOKEN Failure)



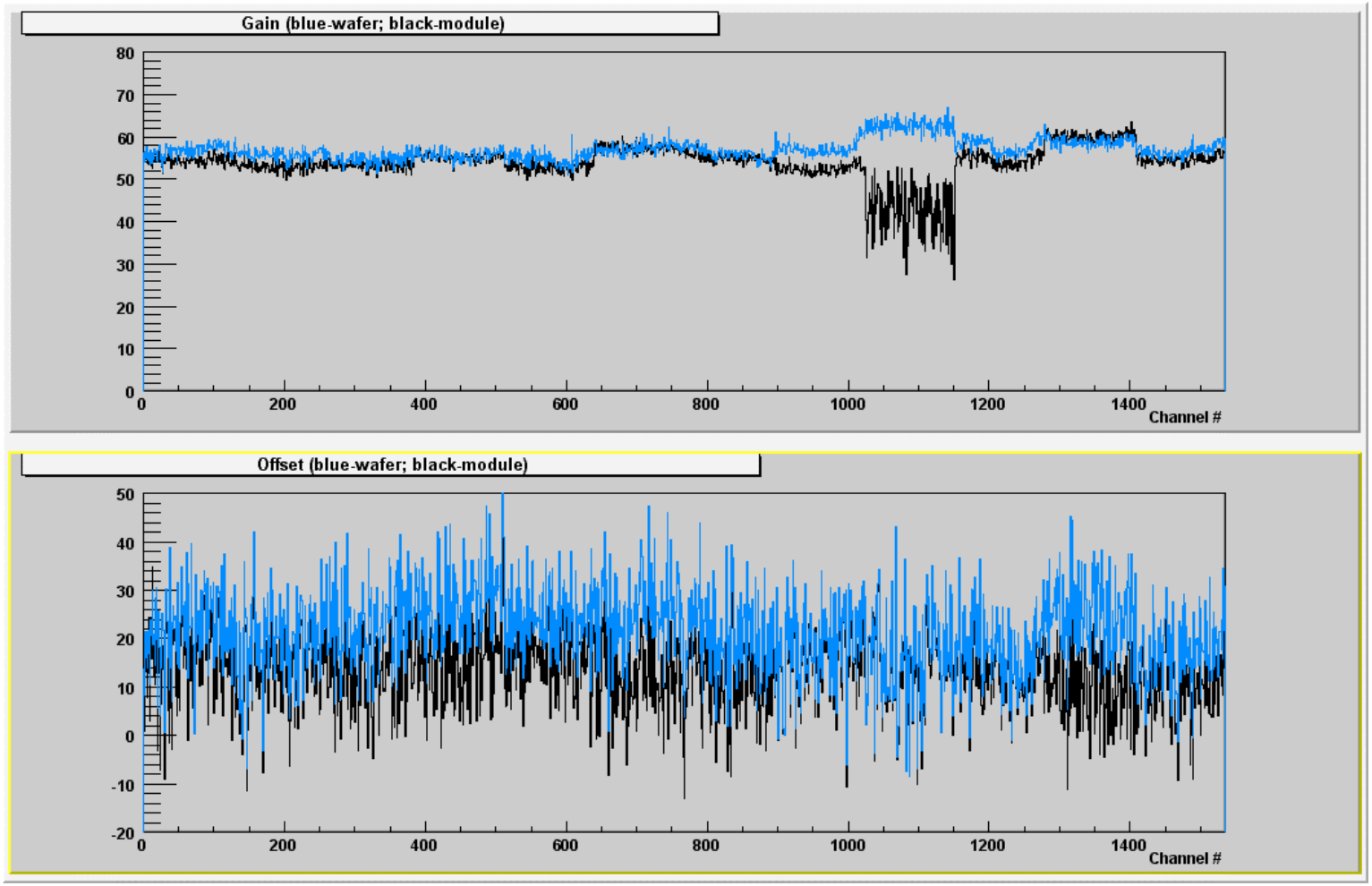
Comparison not available before replacement (data from hybrid overall bad because of token failure)
But wafer data for chip 1 (faulty on hybrid) was normal.

Hybrid 20220040200021
chip 8 Large Gain Spread

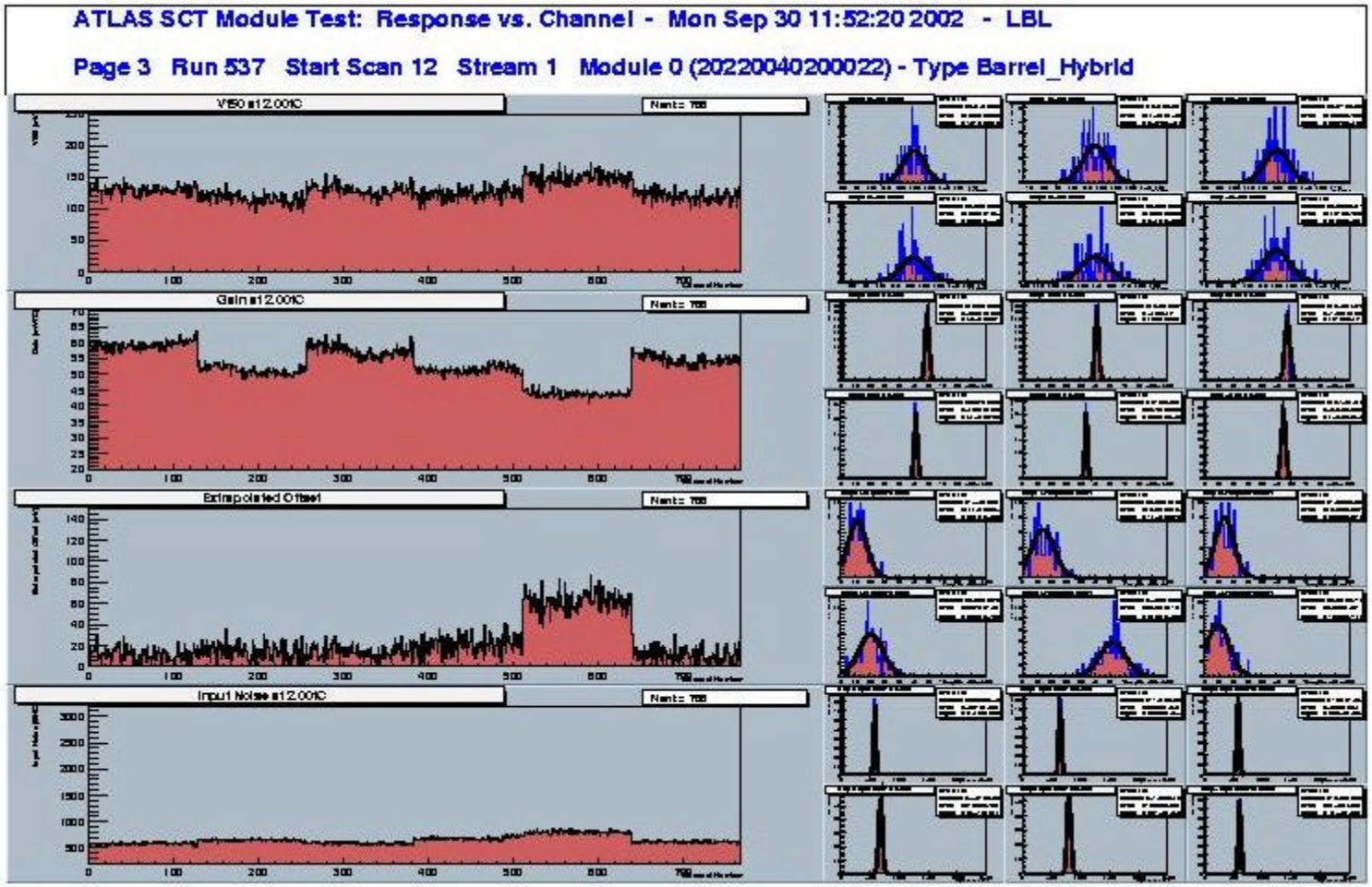


Chip started to work well at Vcc=3.7V - Voltage drop at the hybrid 50 mV
Under wafer test (test performed at UCSC) works at nominal Vcc

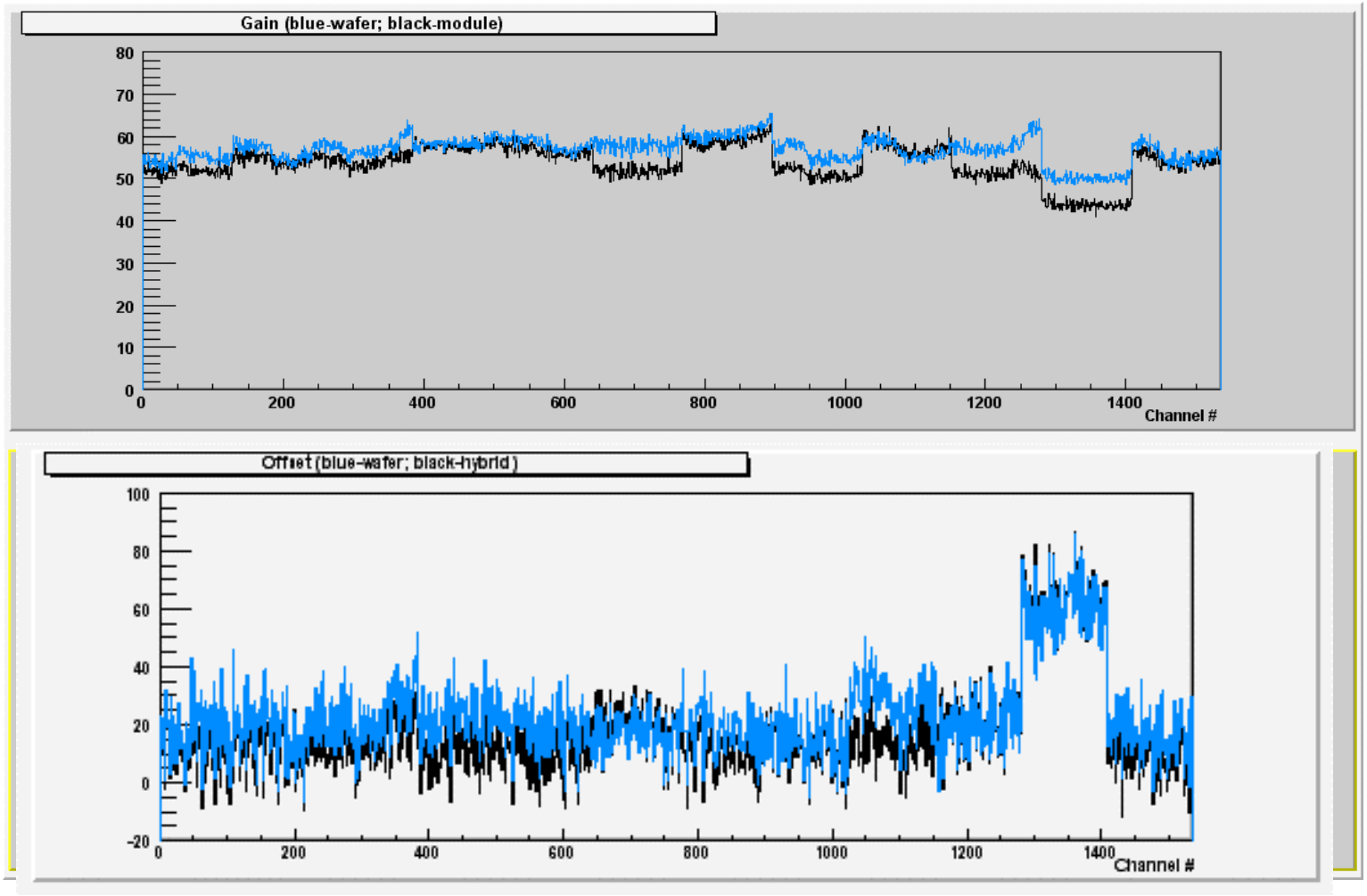
Hybrid 20220040200021
Wafer/Hybrid Comparison



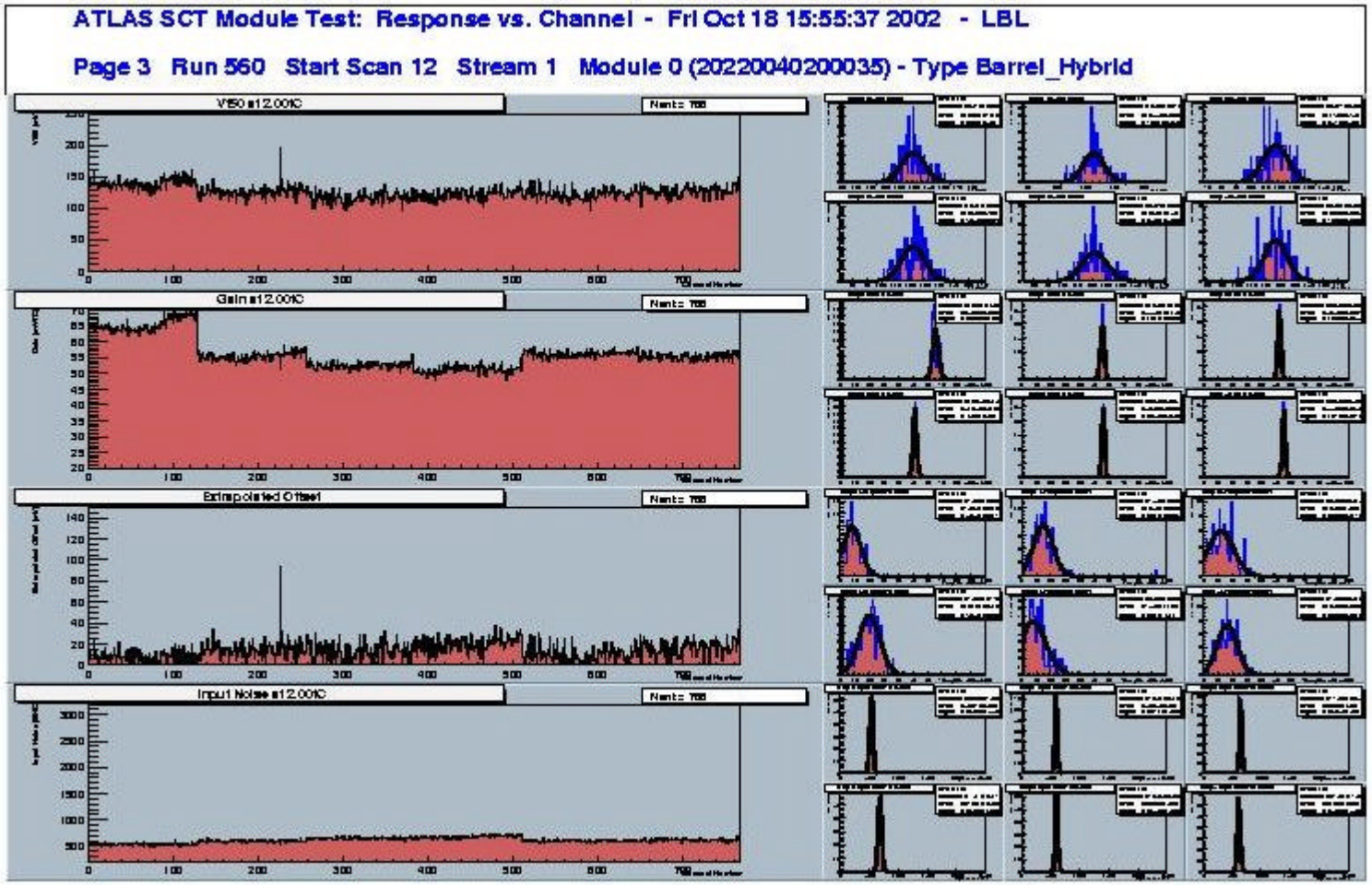
Hybrid 20220040200022
Chip 10 High Offset



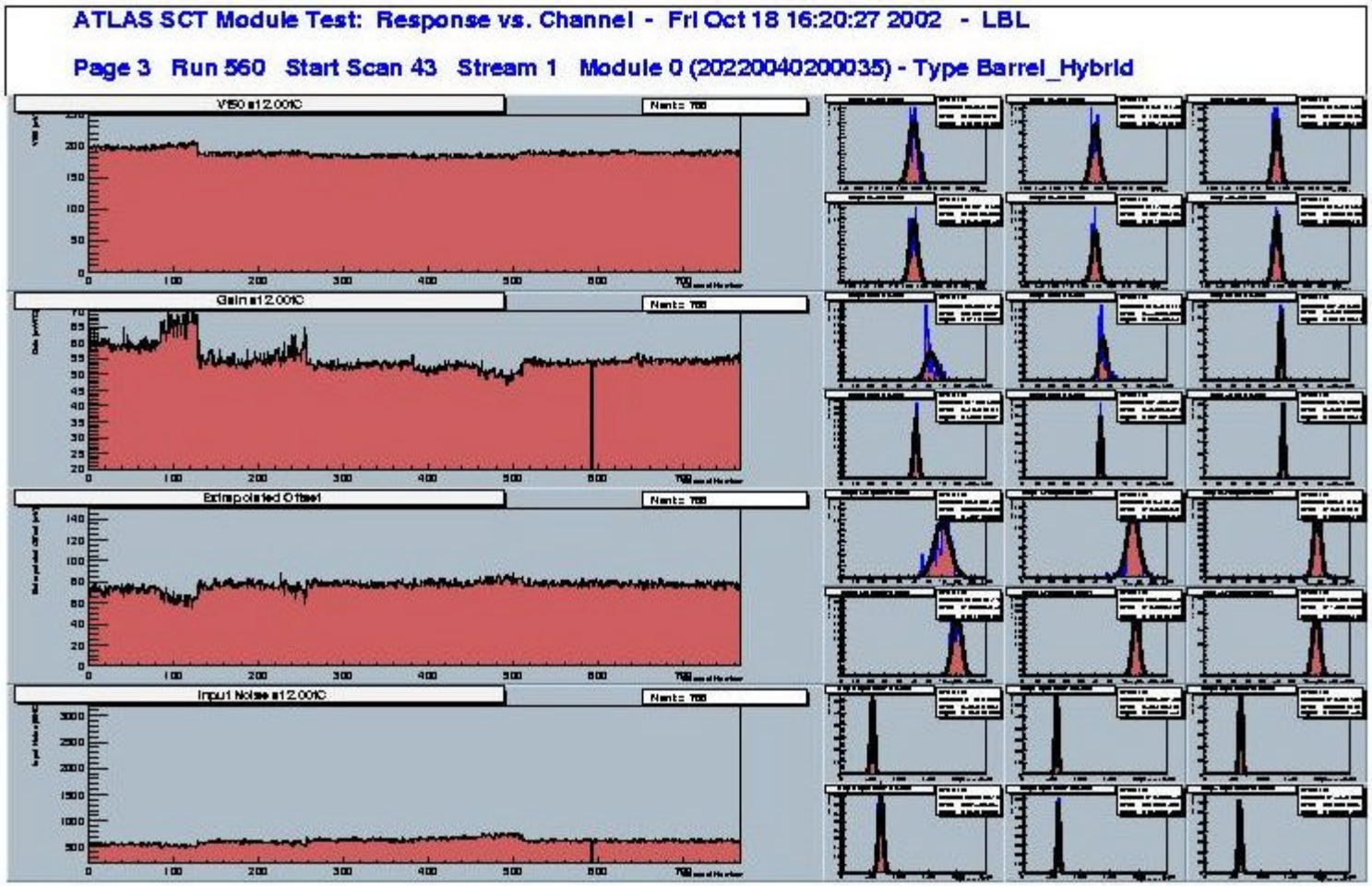
Hybrid 2022004020002 2
Wafer/Hybrid Comparison



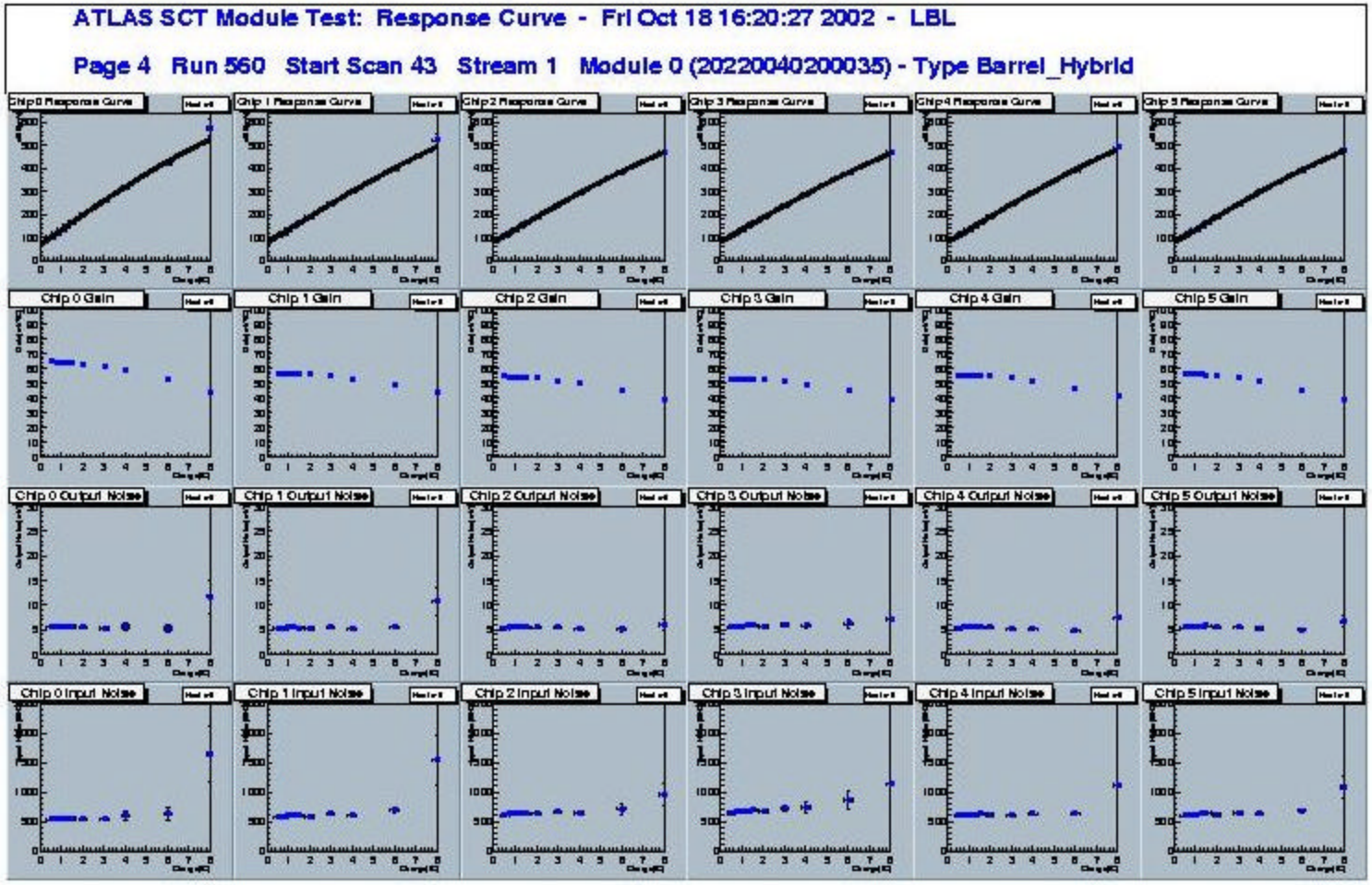
Hybrid 20220040200035
Chip 6 (M8) High Gain (3Pt)



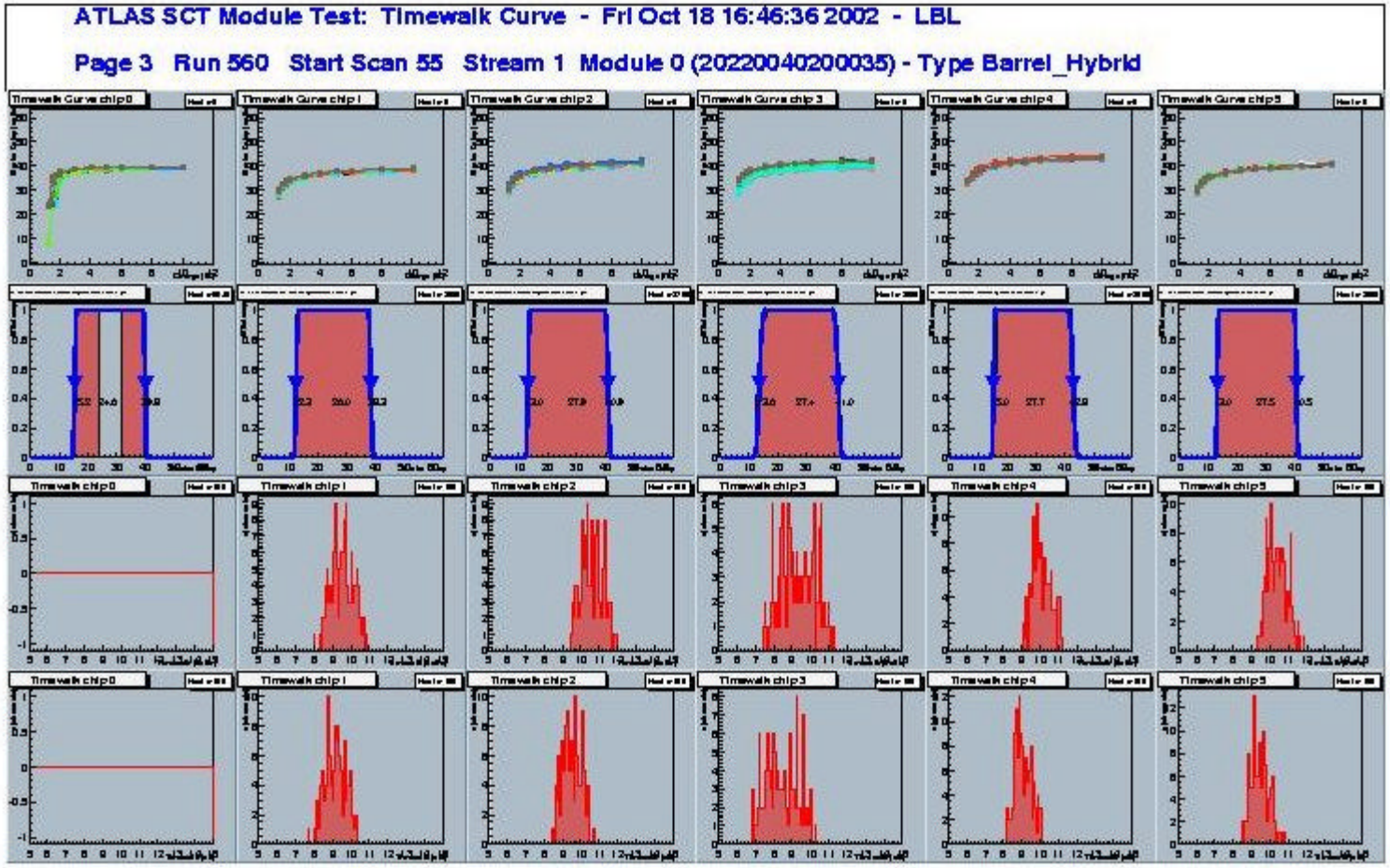
Hybrid 20220040200035
Chip 6 (M8) High Gain (After trim)



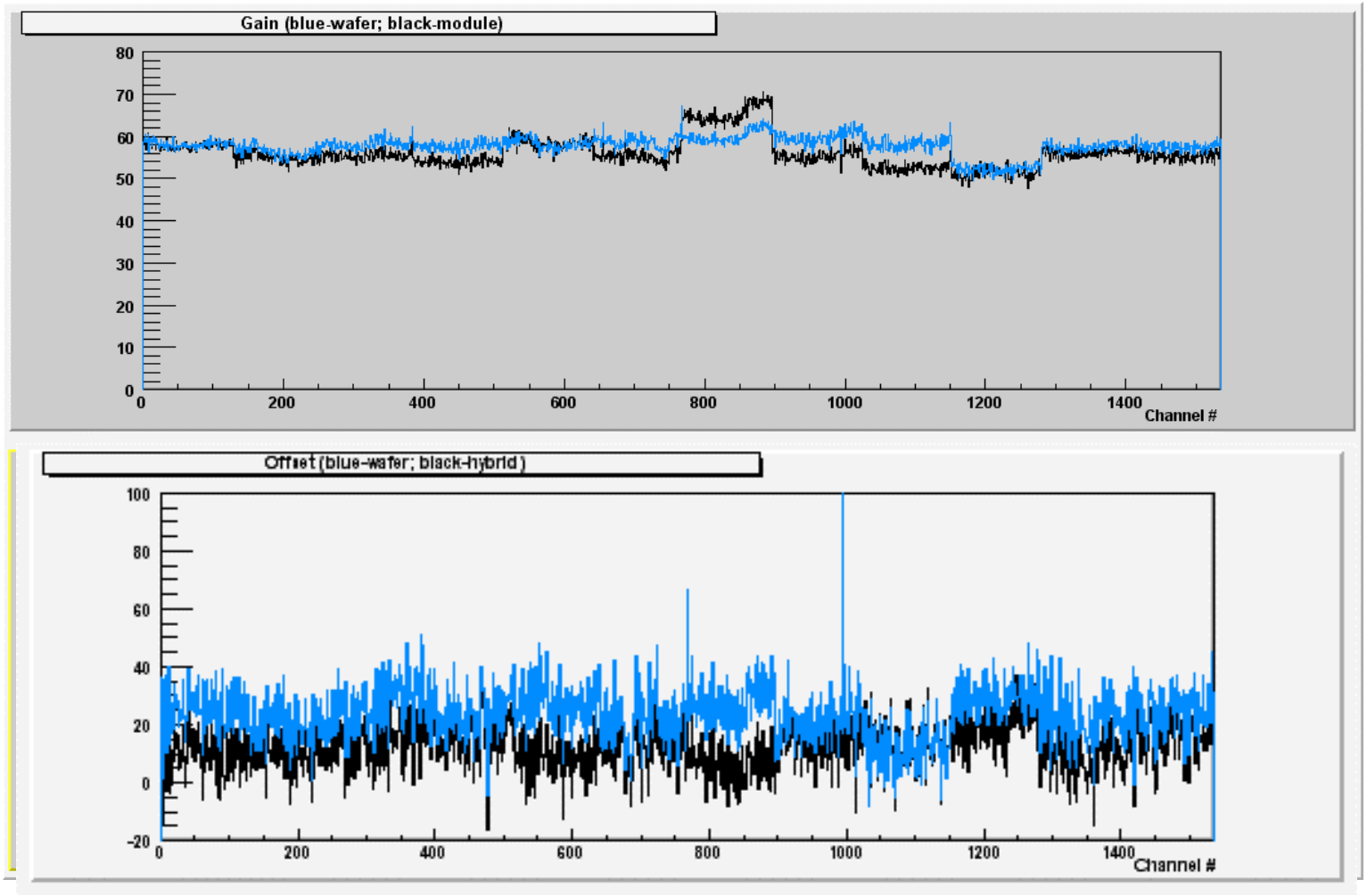
Hybrid 20220040200035
Chip 6 (M8) High Gain (after trim)



Hybrid 20220040200035
Chip 6 (M8) Time Walk Failure

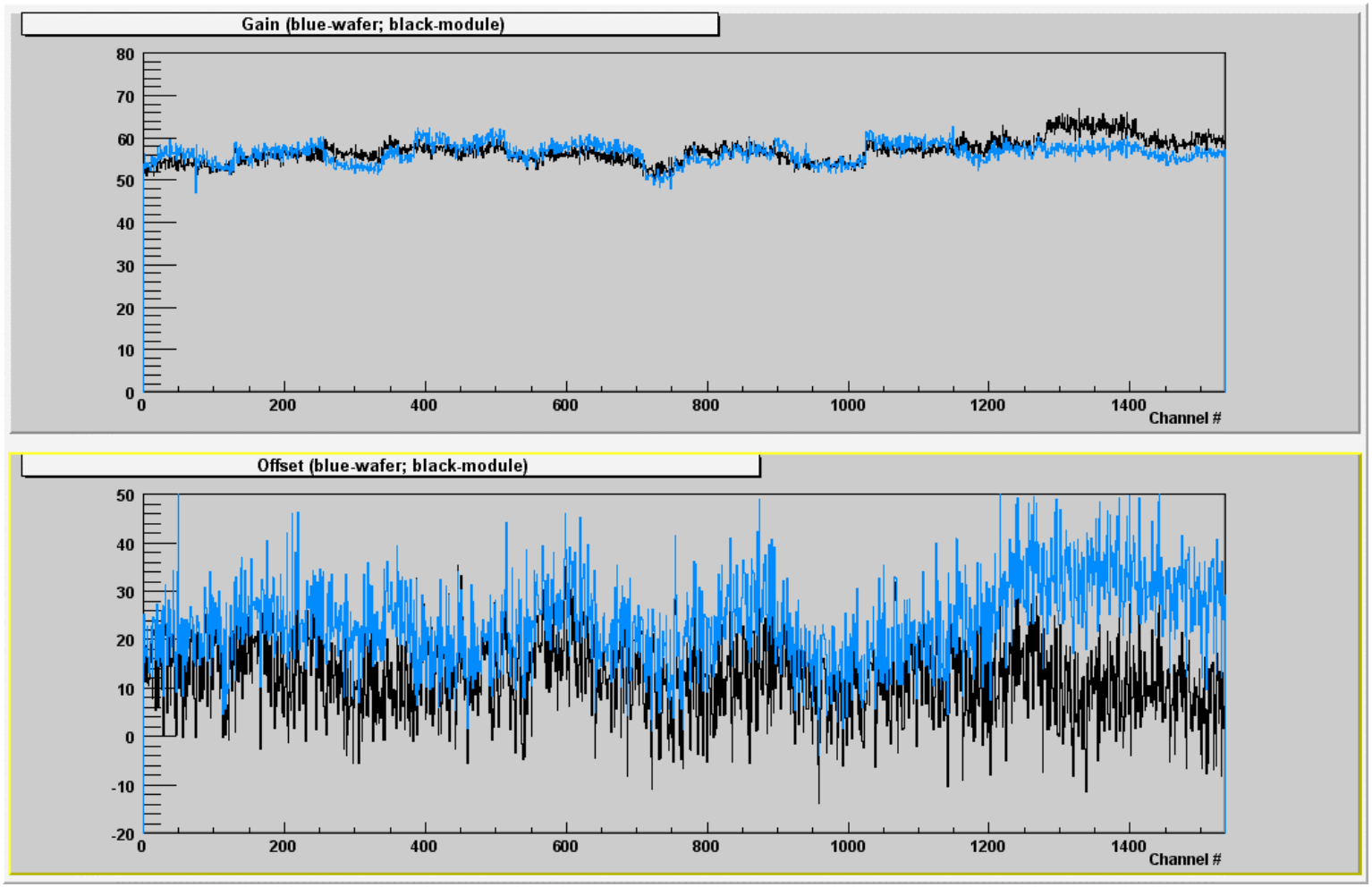


Hybrid 2022040200035
Wafer/Hybrid Comparison

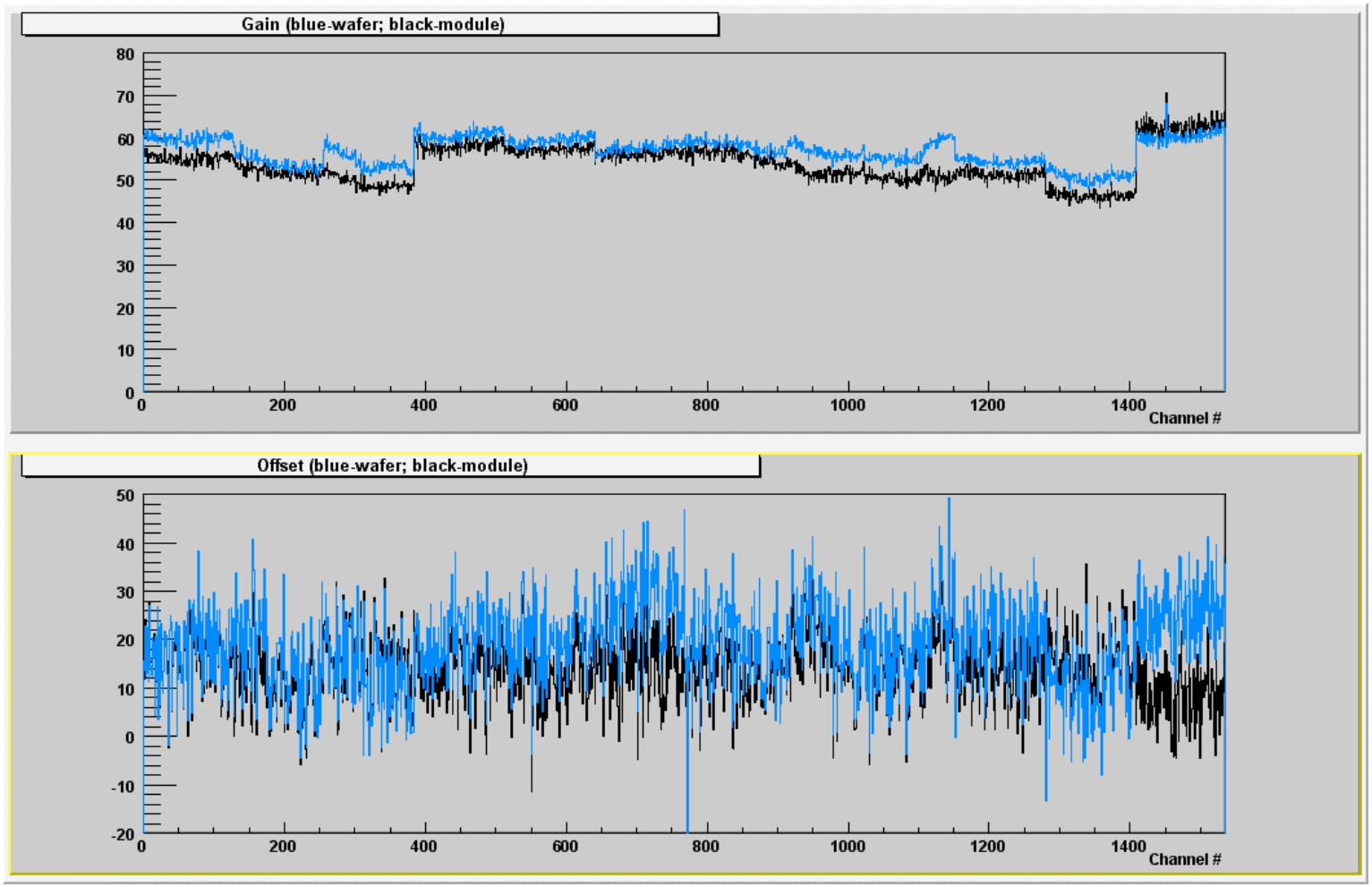


Gain (non) uniformity 

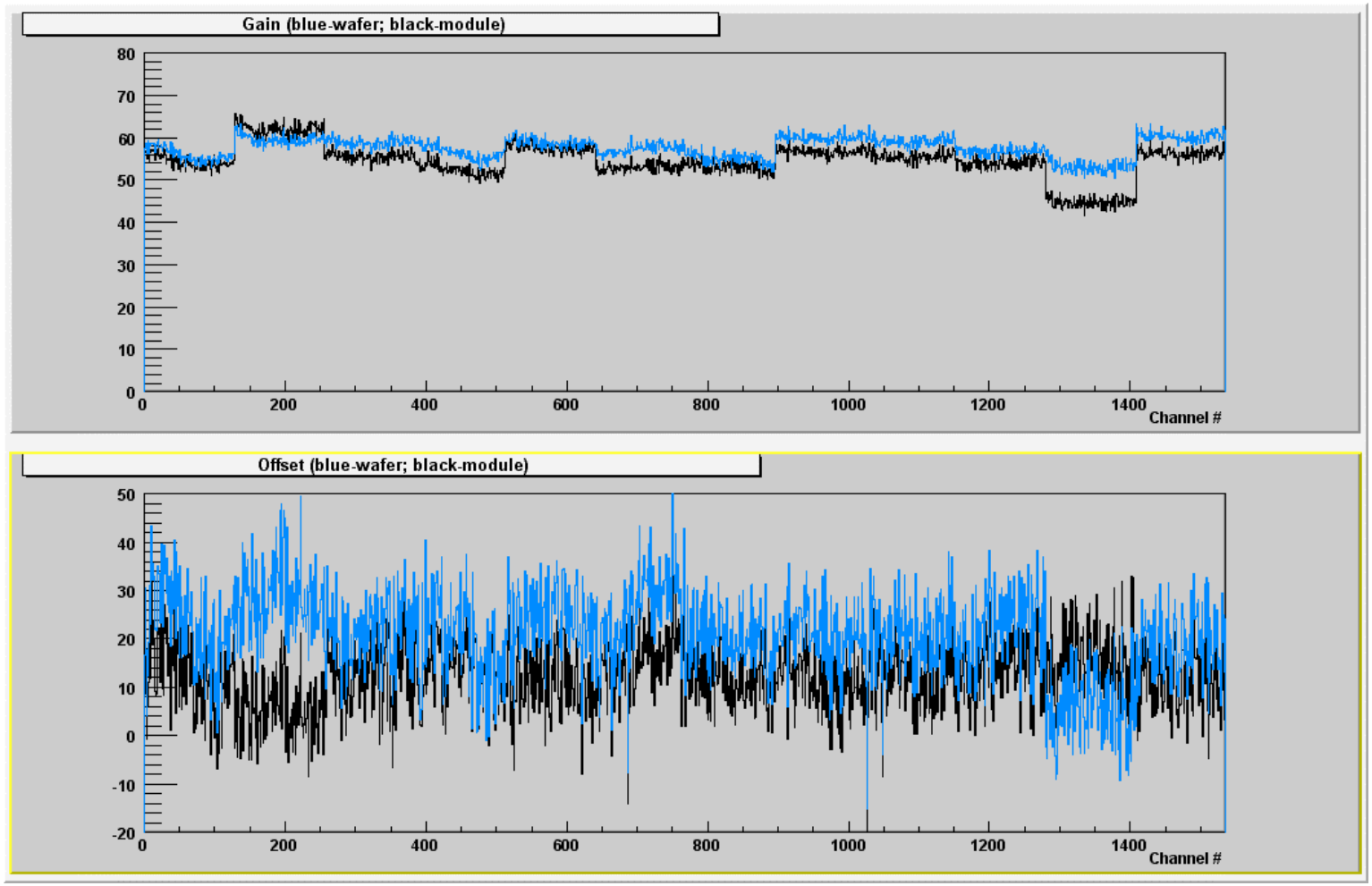
Wafer/Hybrid Comparison
Hybrid 2022004020008



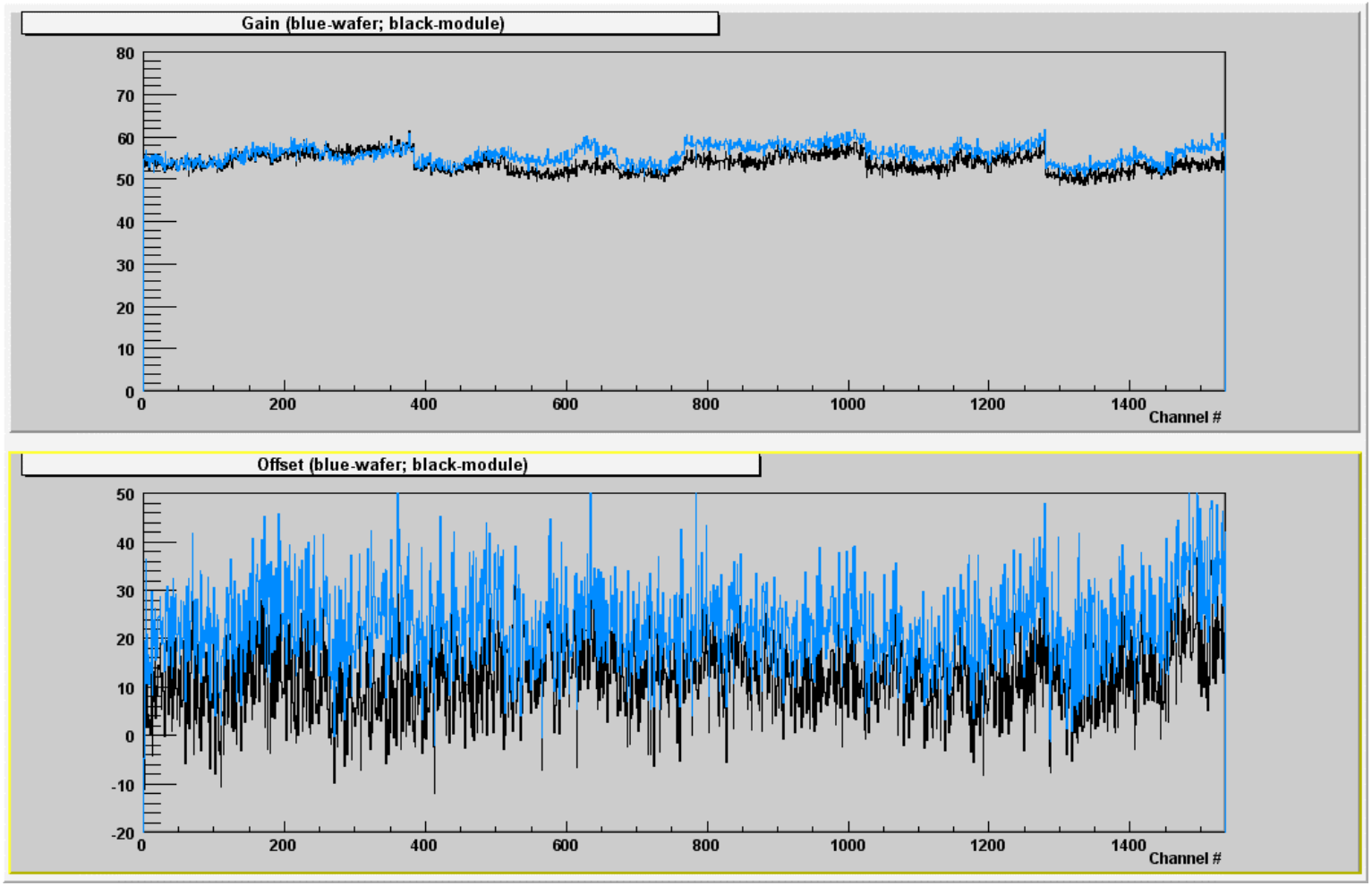
Wafer/Hybrid Comparison
Hybrid 20220040200015



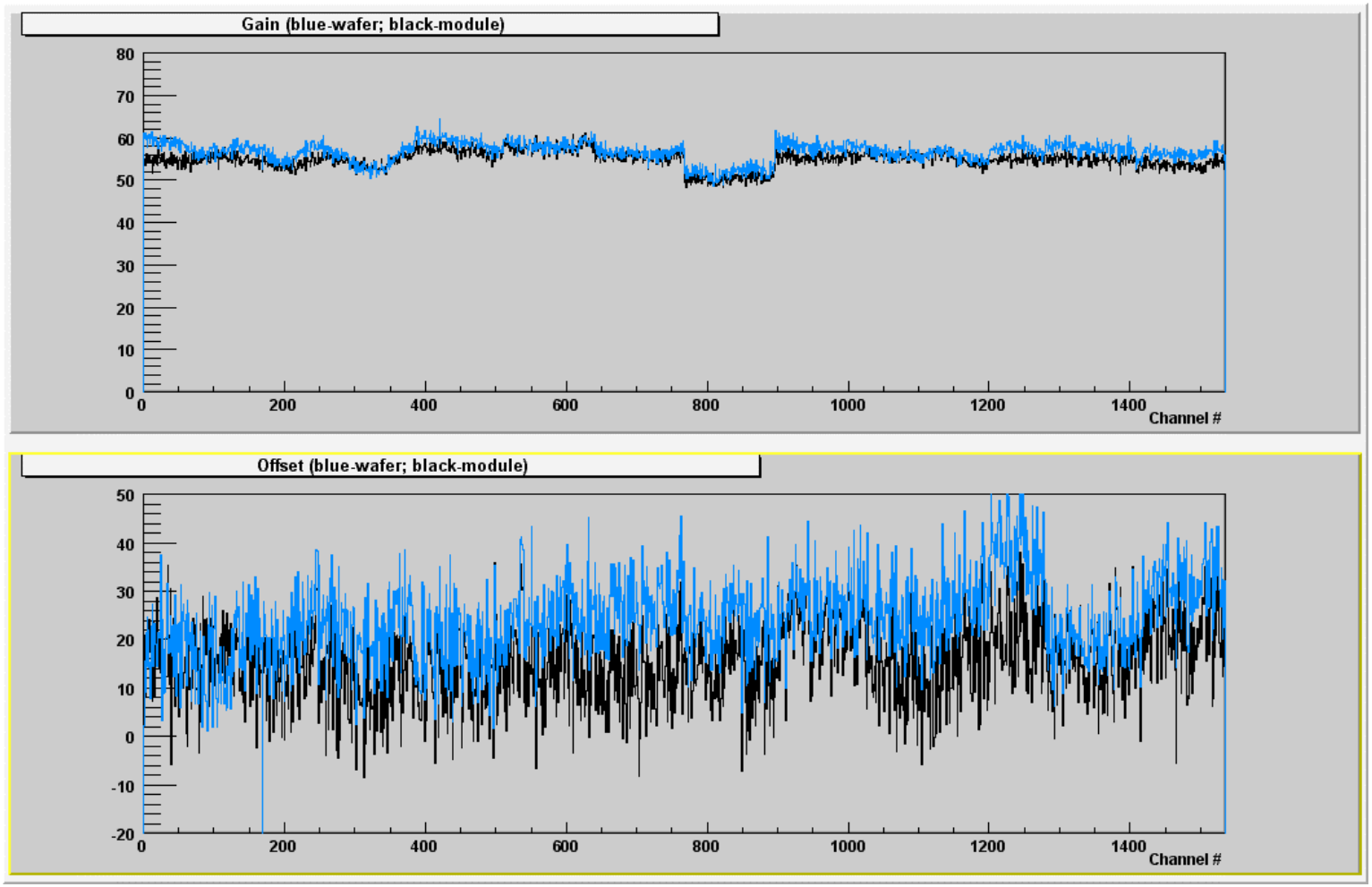
Wafer/Hybrid Comparison
Hybrid 2022004020029



Wafer/Hybrid Comparison
Hybrid 20220040200030



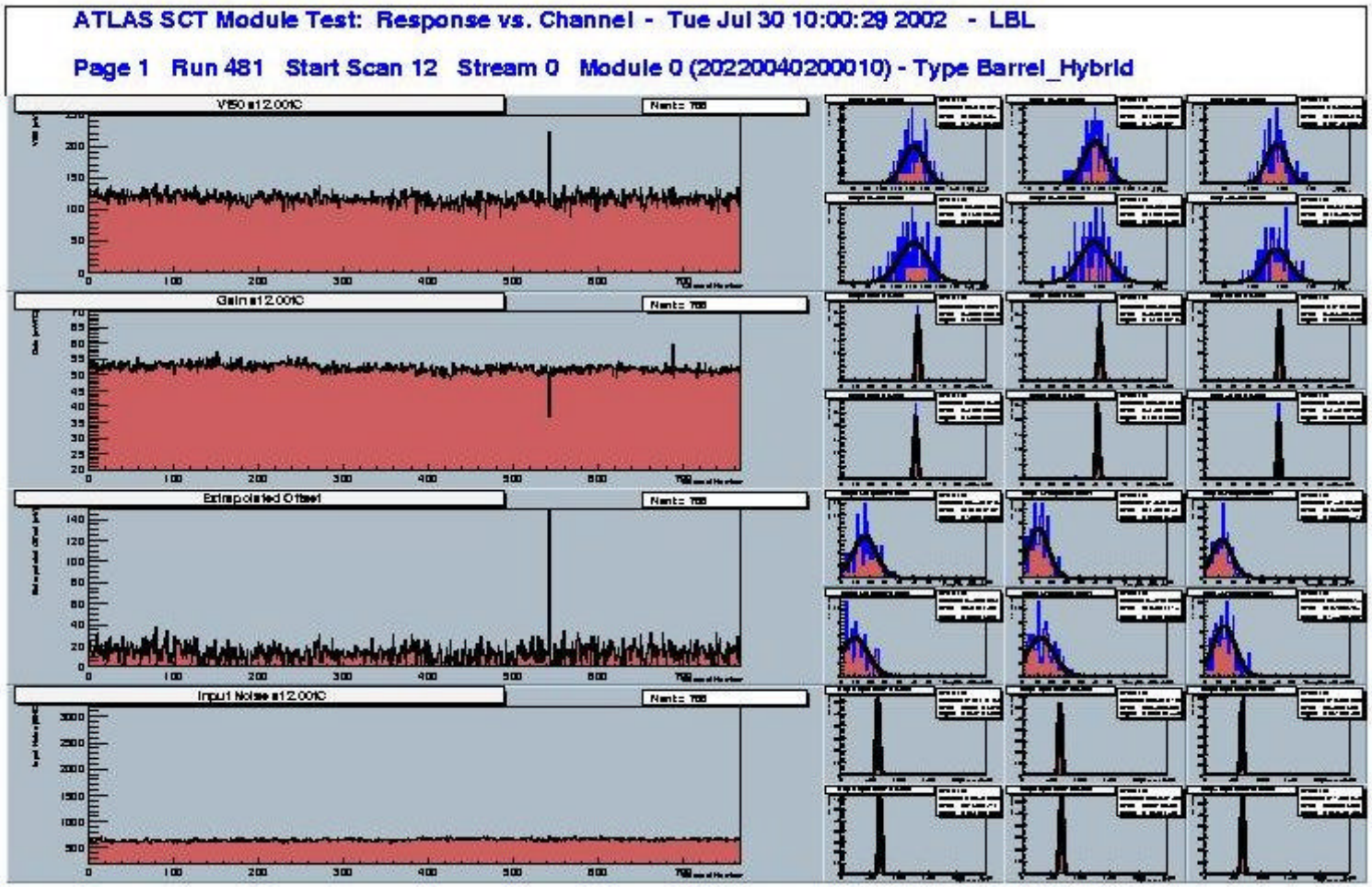
Wafer/Hybrid Comparison
Hybrid 2022004020003 3



High Offset (low gain) 

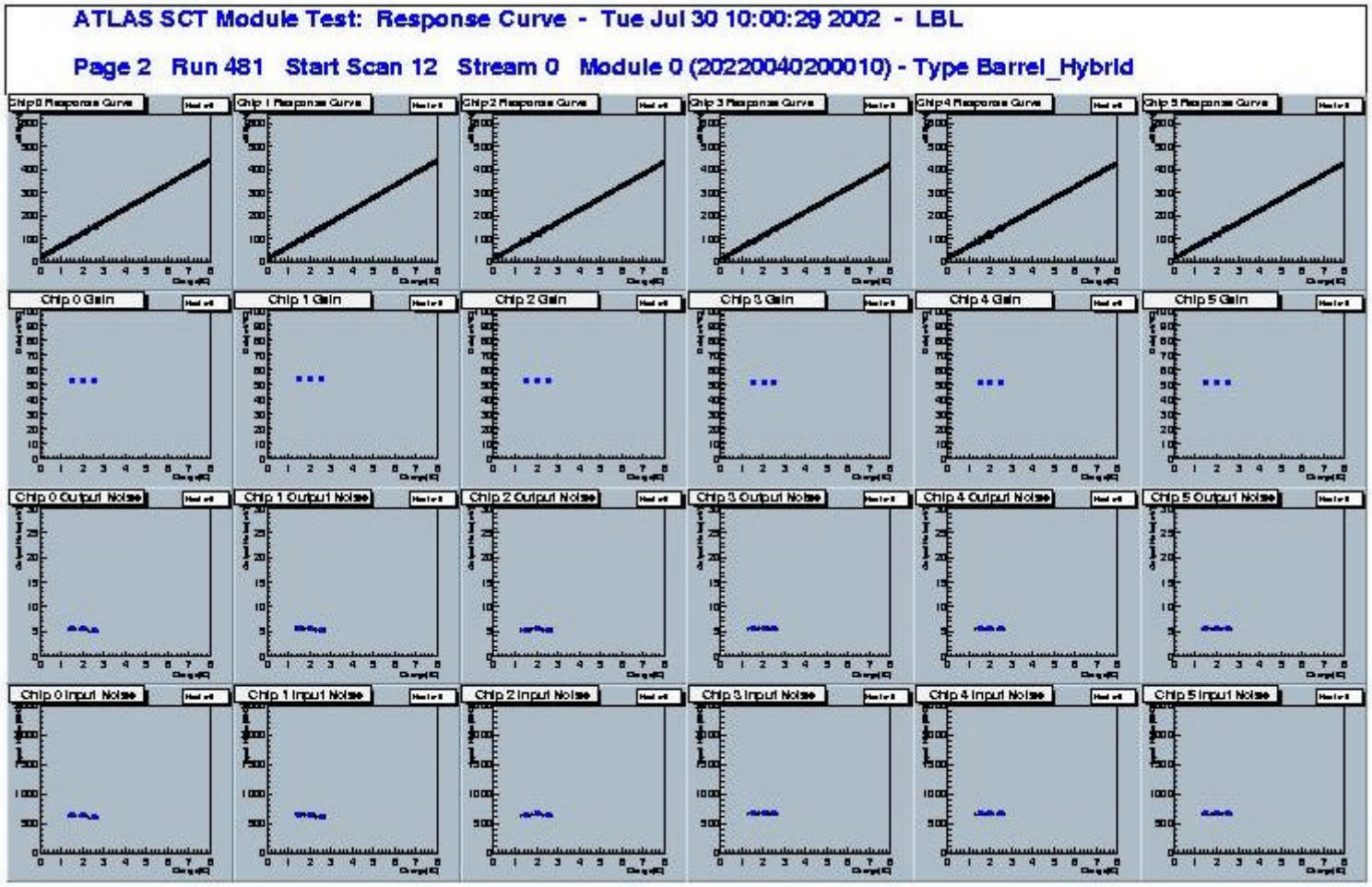
Hybrid 20220040200010

High Offset (low gain)



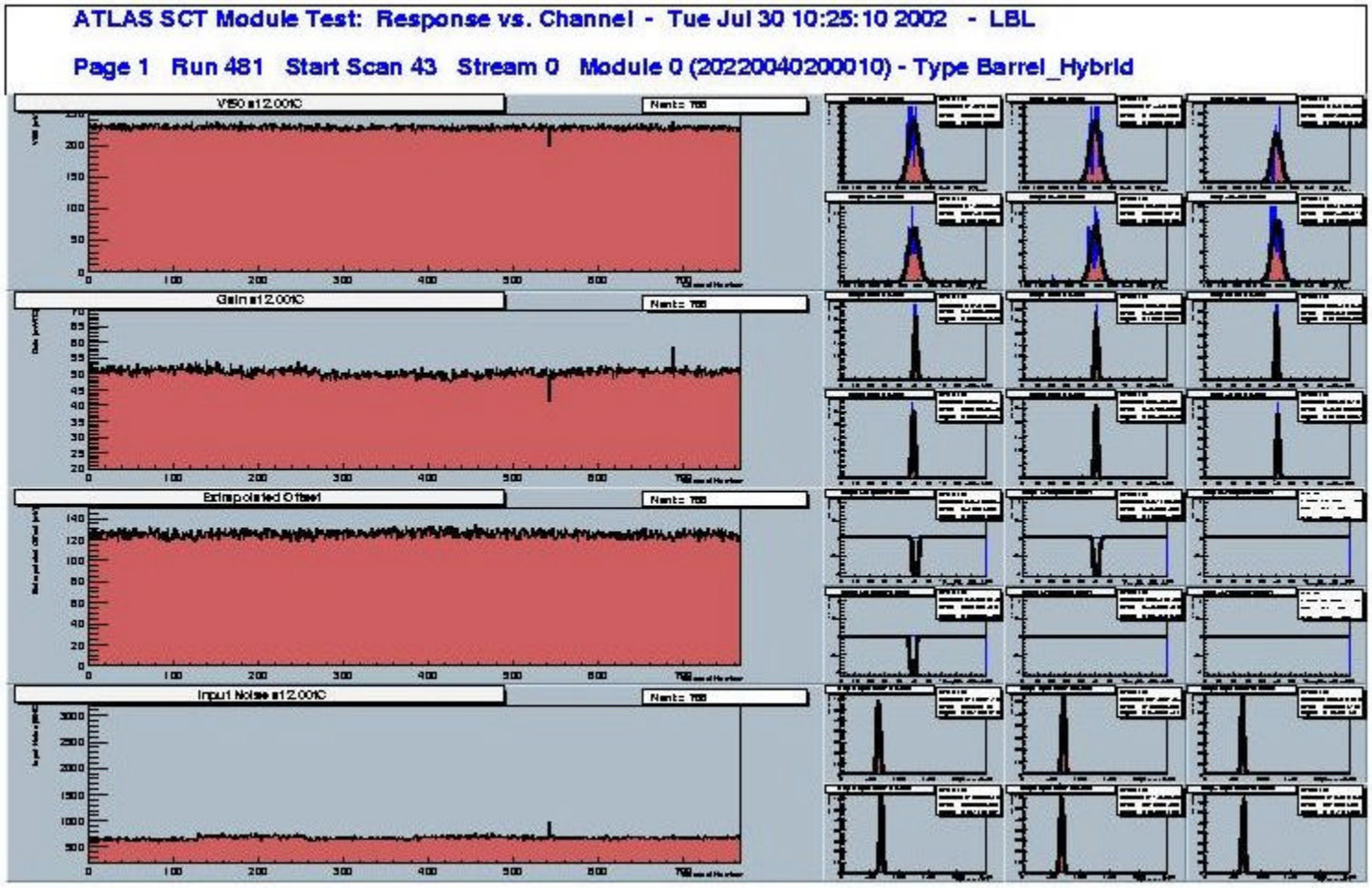
Hybrid 20220040200010

High Offset (low gain)



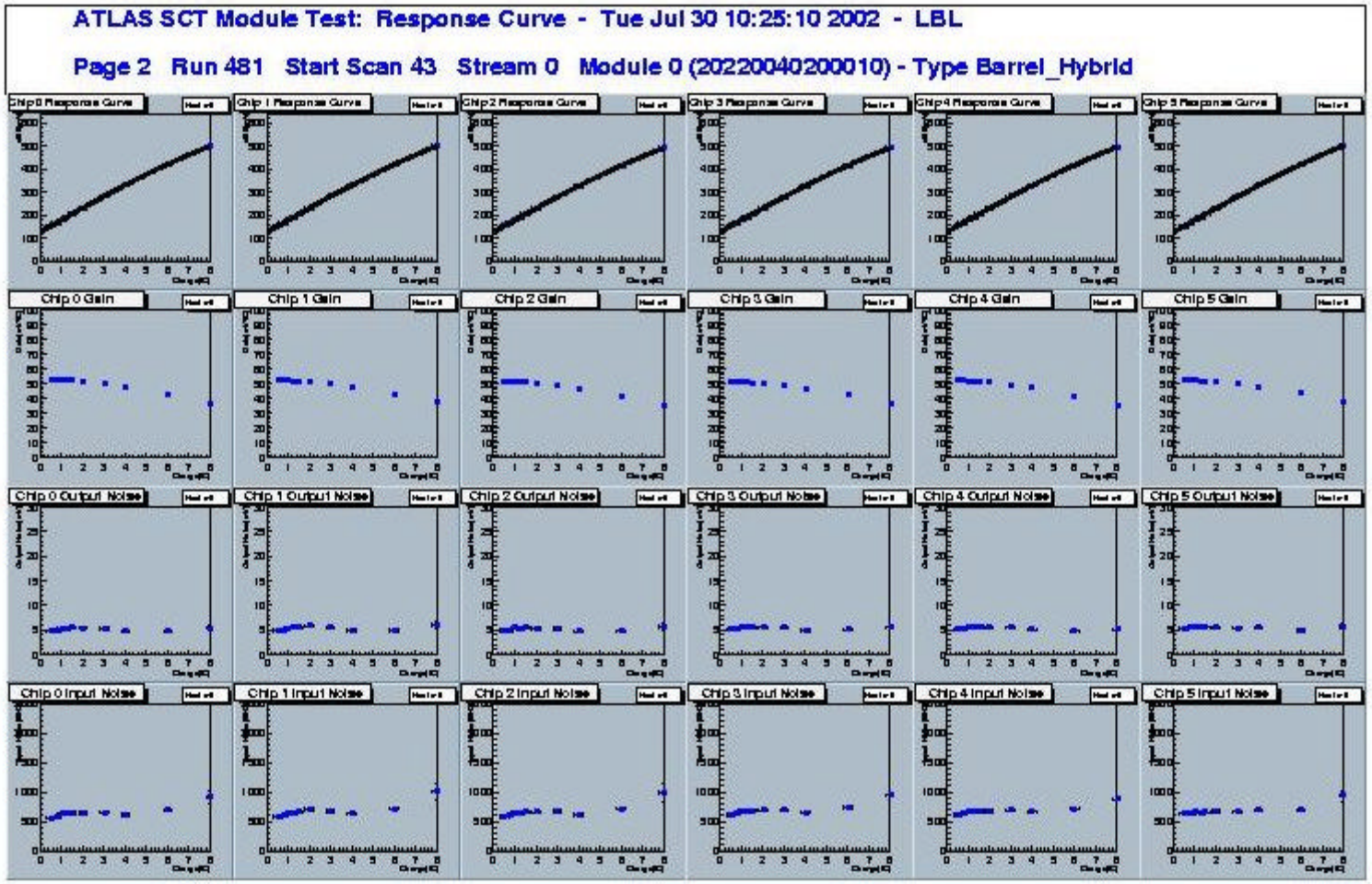
Hybrid 20220040200010

High Offset (low gain)

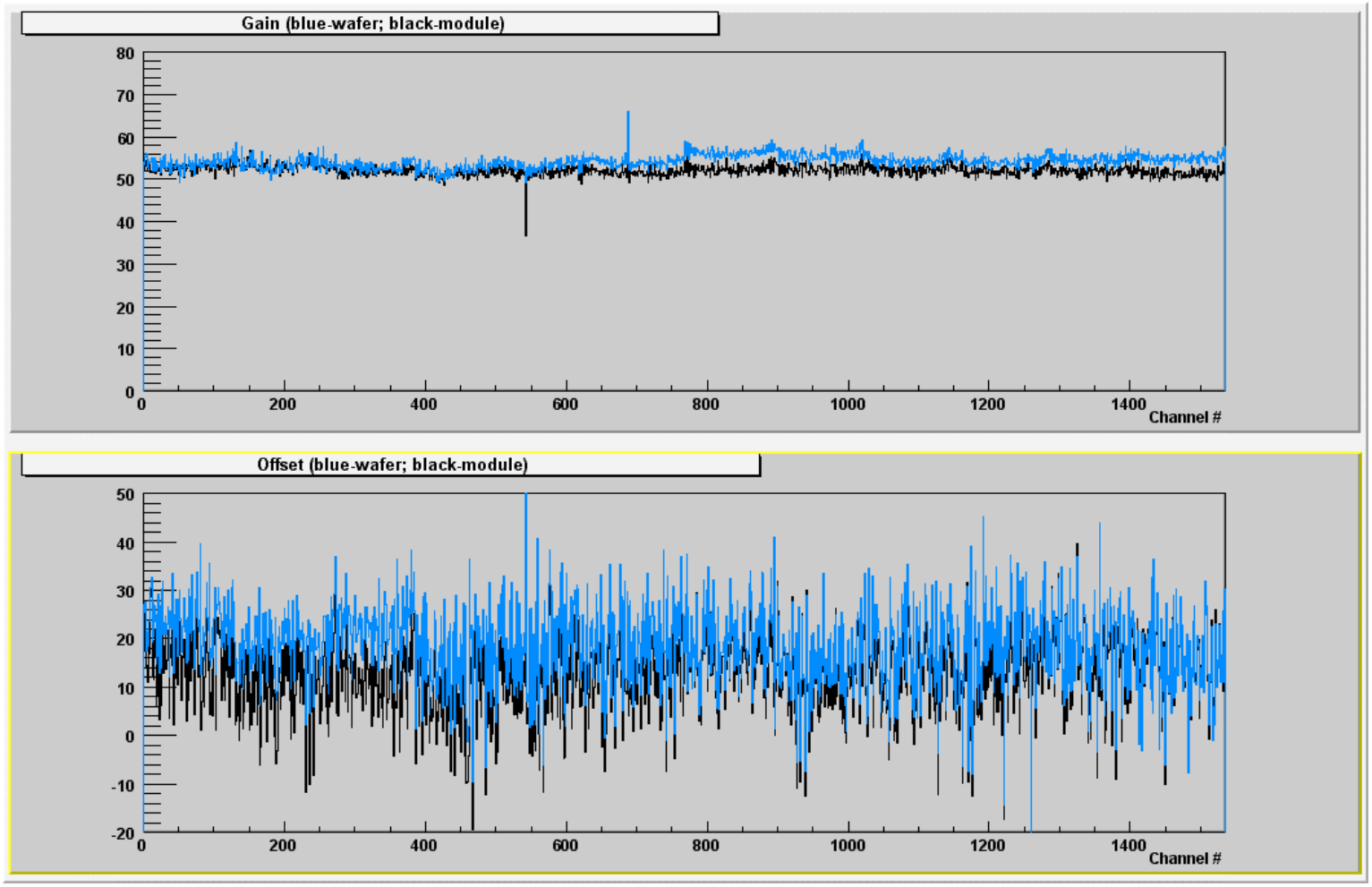


Hybrid 20220040200010

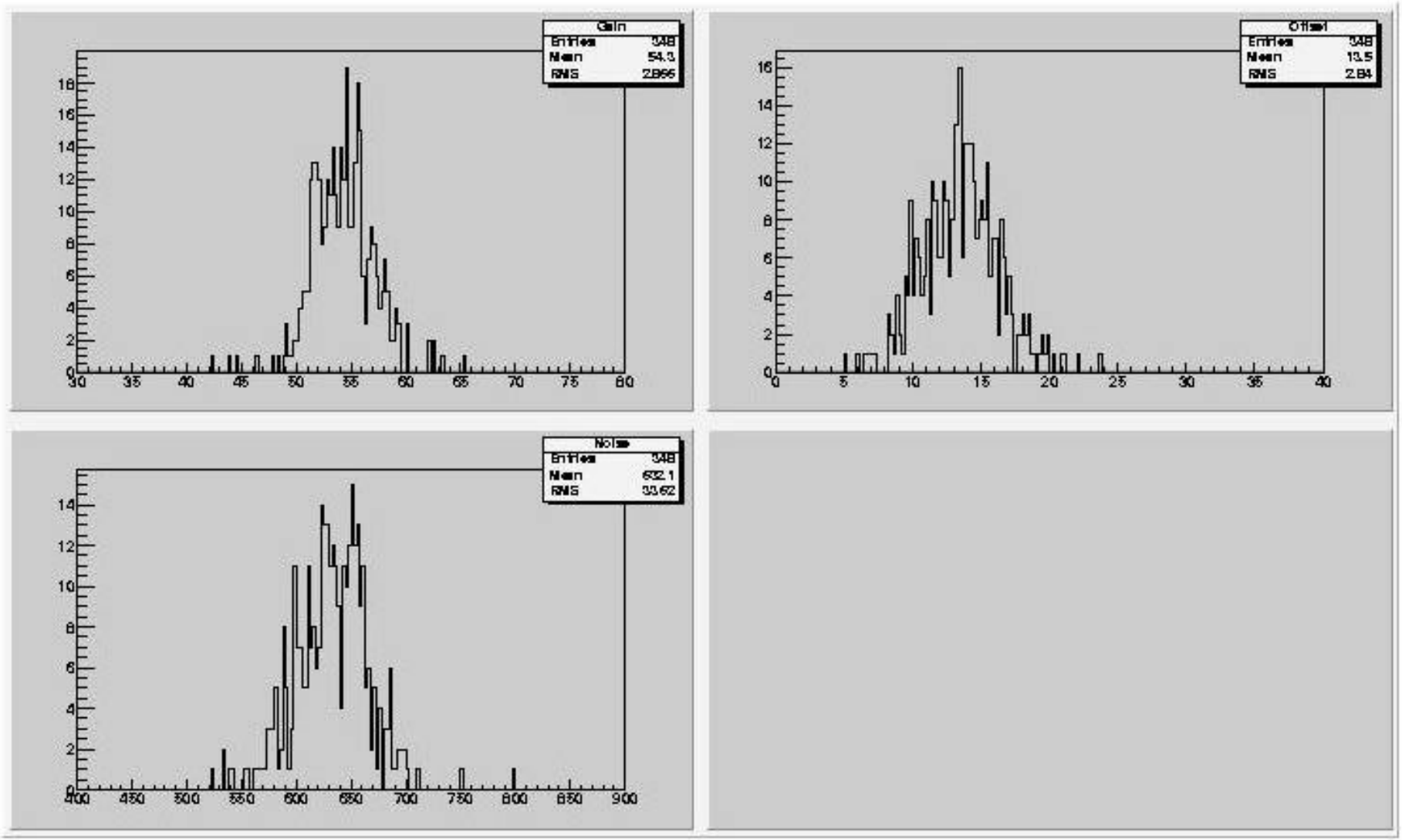
High Offset (low gain)



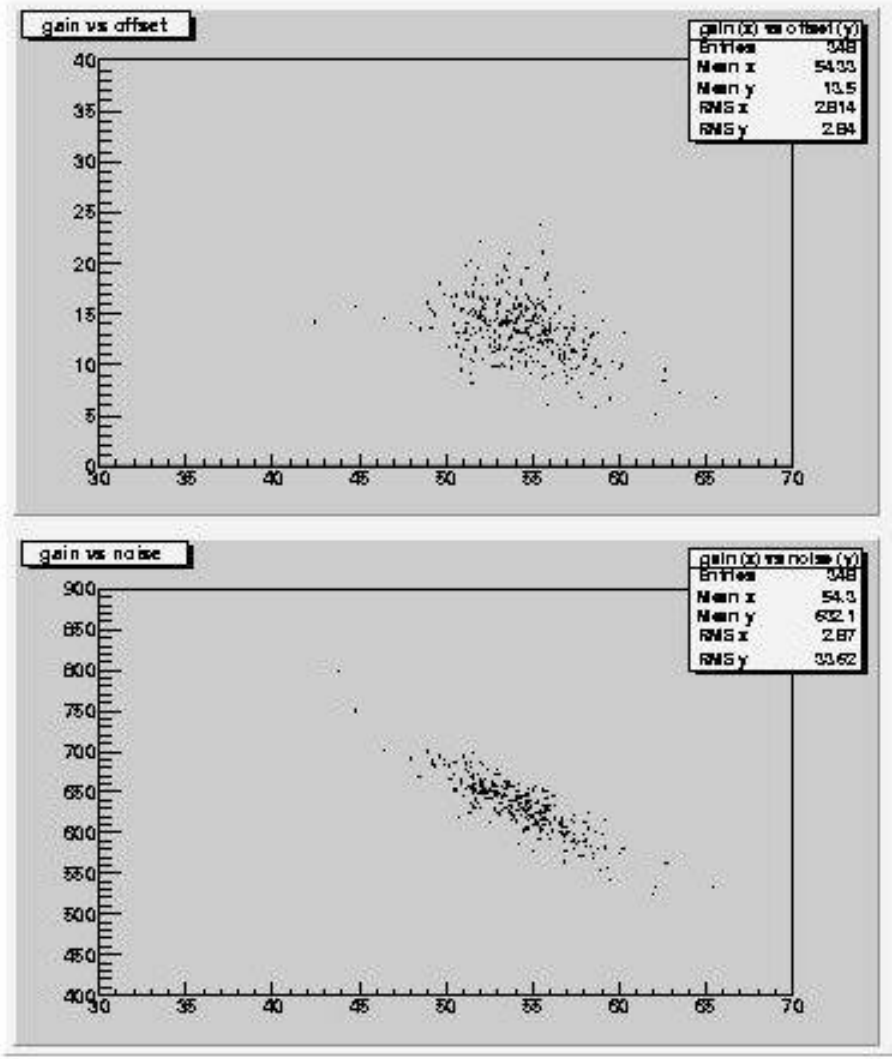
Wafer/Hybrid Comparison
Hybrid 20220040200010



Gain/Offset/Noise Distribution



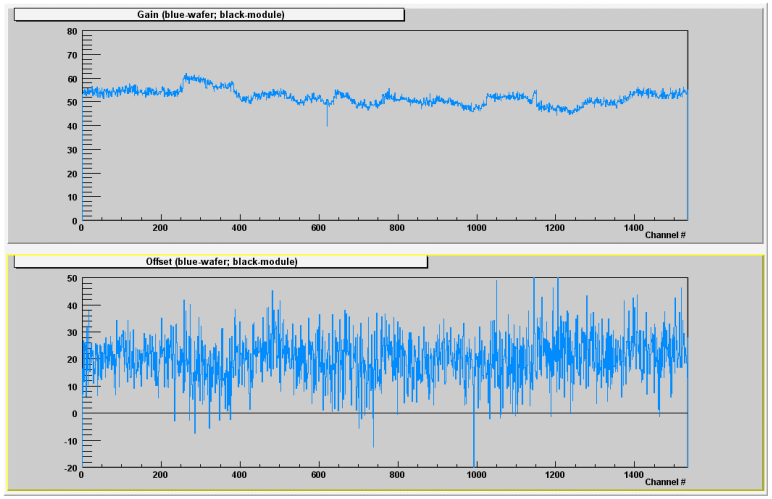
Gain/Offset/Noise Correlation



Wafer Data

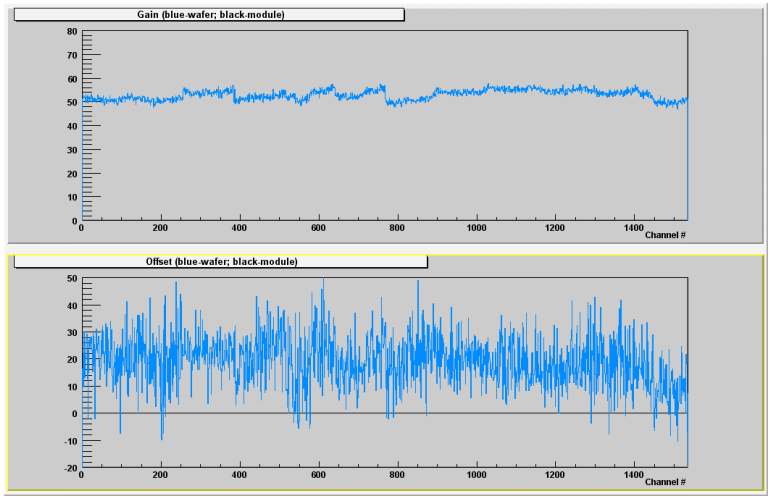
Pure Wafer data for chips available to use (still in the gel pack)
It could be useful is need to match chips before placing on hybrid

z40802-w09



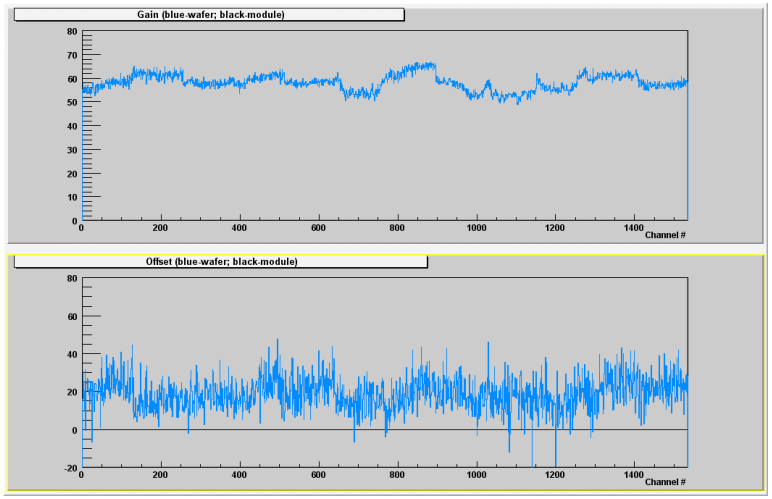
1

z40802-w09



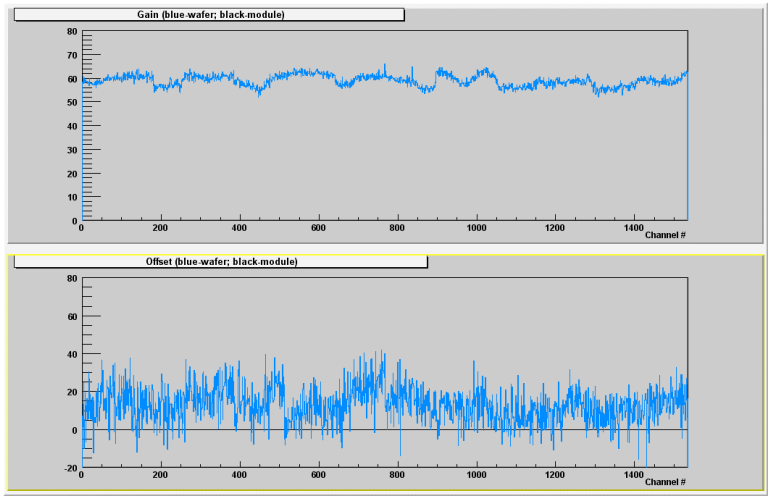
2

z40802-w11



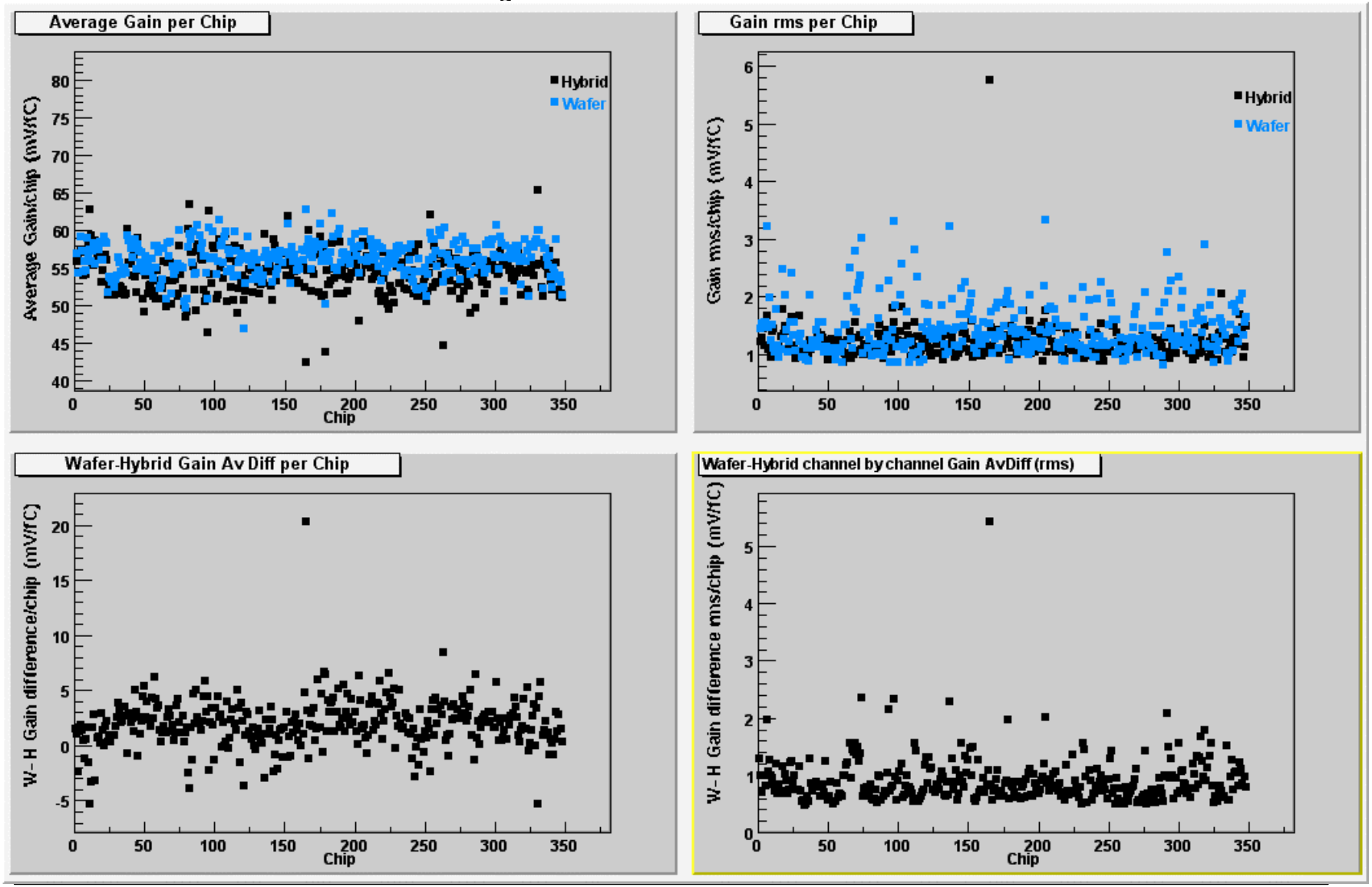
4

z40802-w11

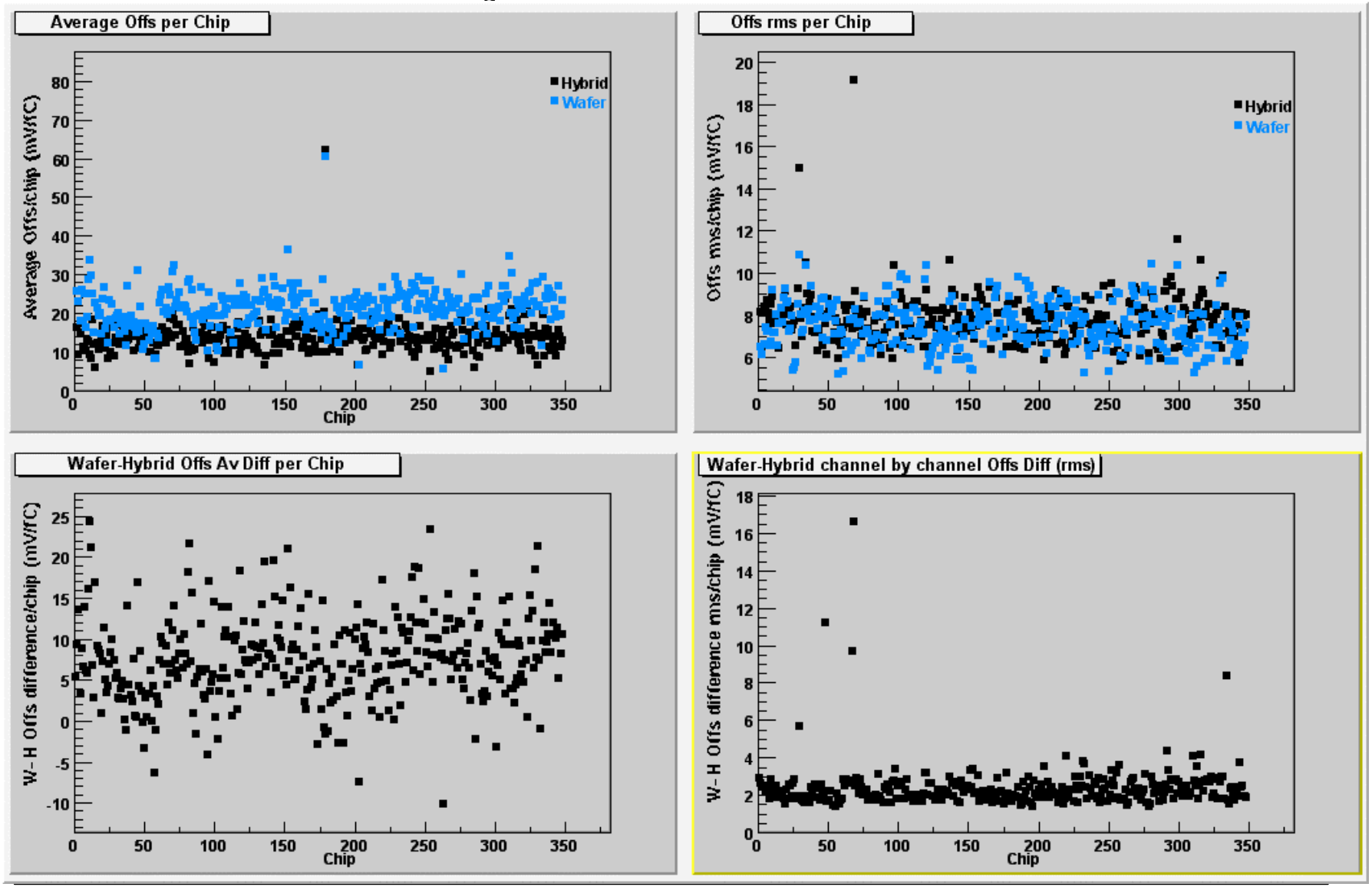


6

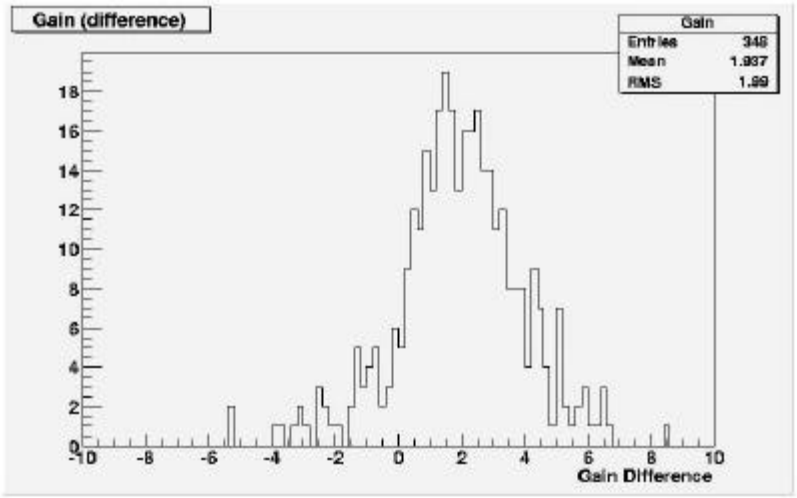
Wafer/Hybrid Correlation - Gain

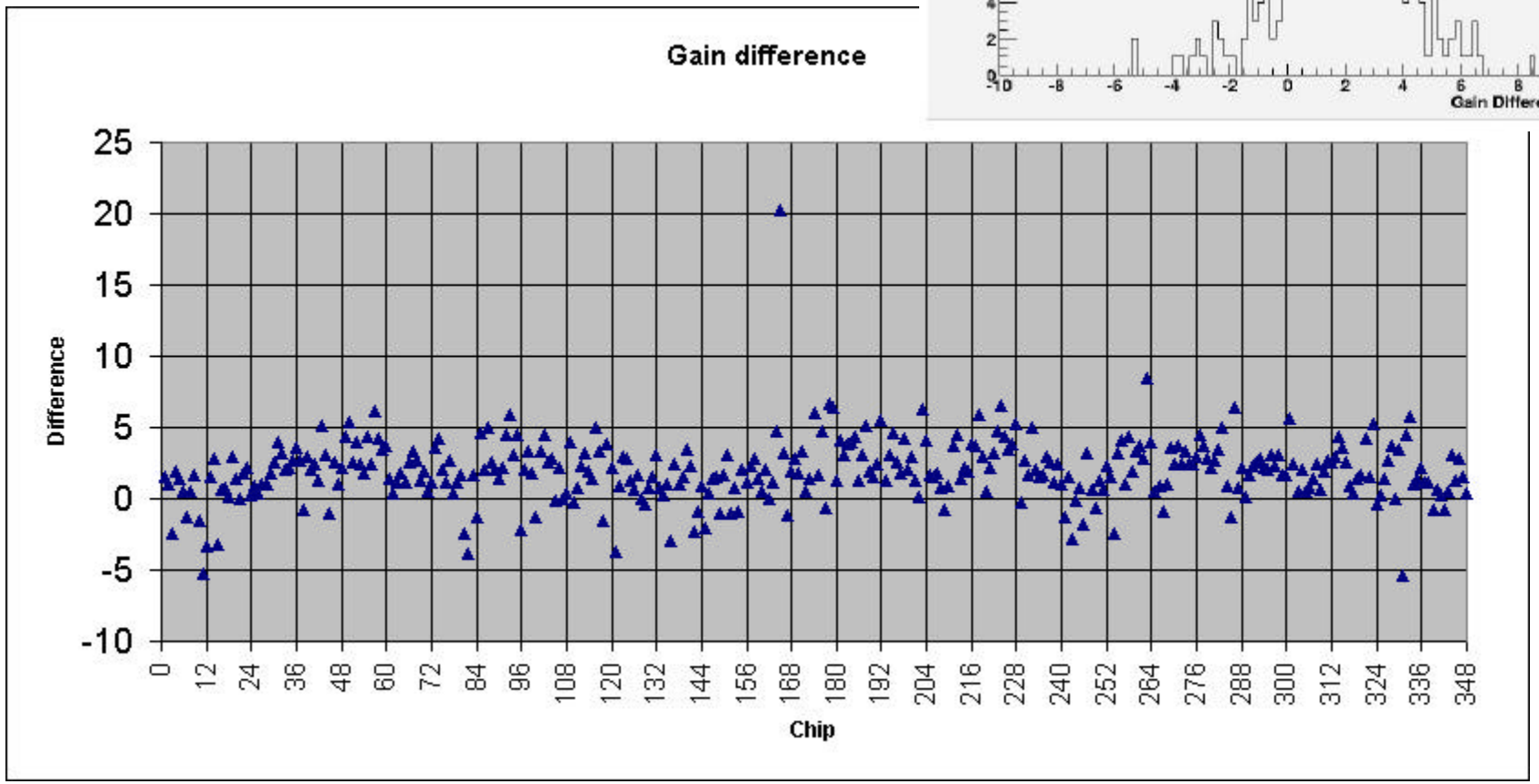


Wafer/Hybrid Correlation - Offset



Wafer/Hybrid Correlation
Average Gain Difference

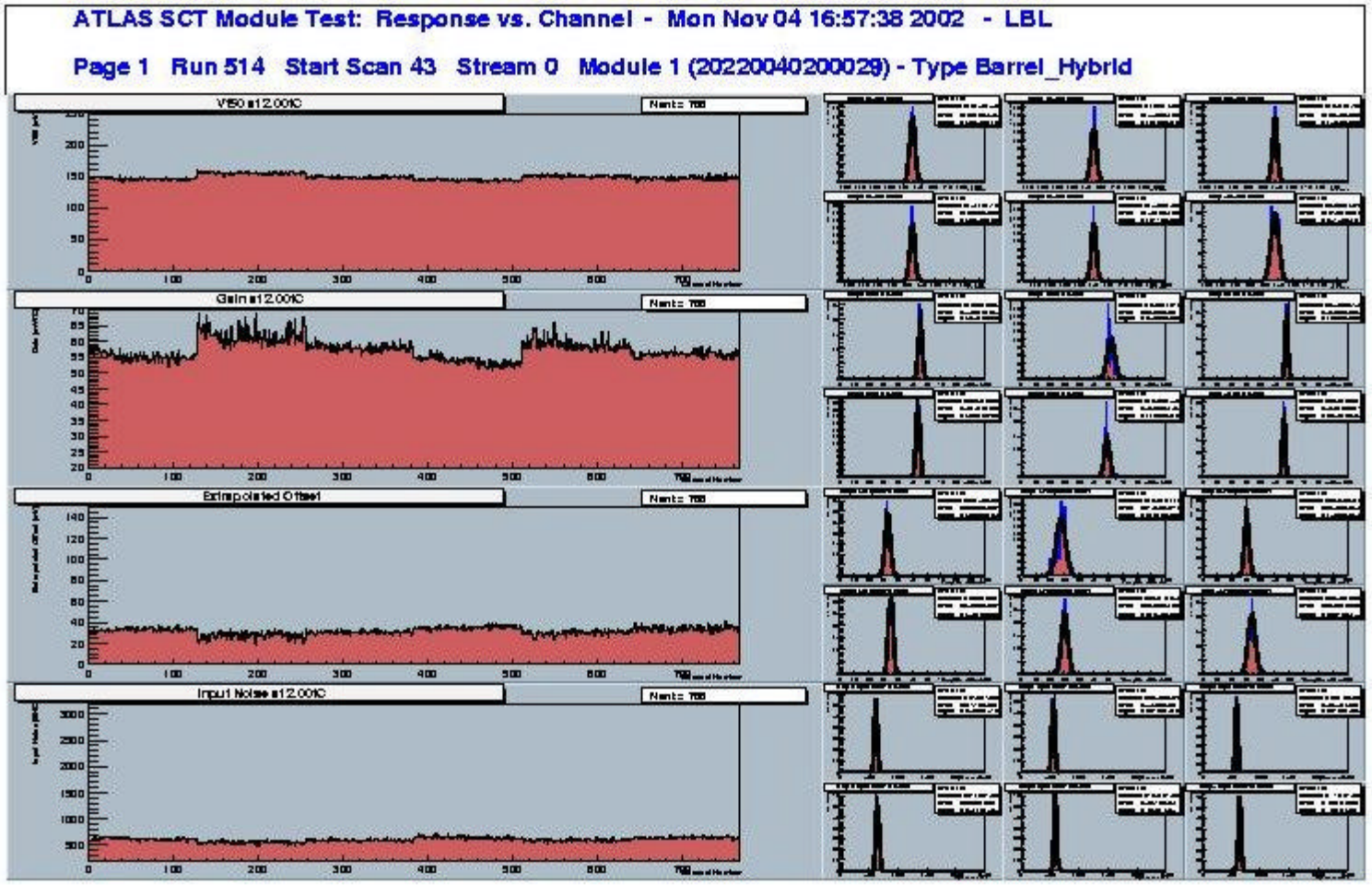




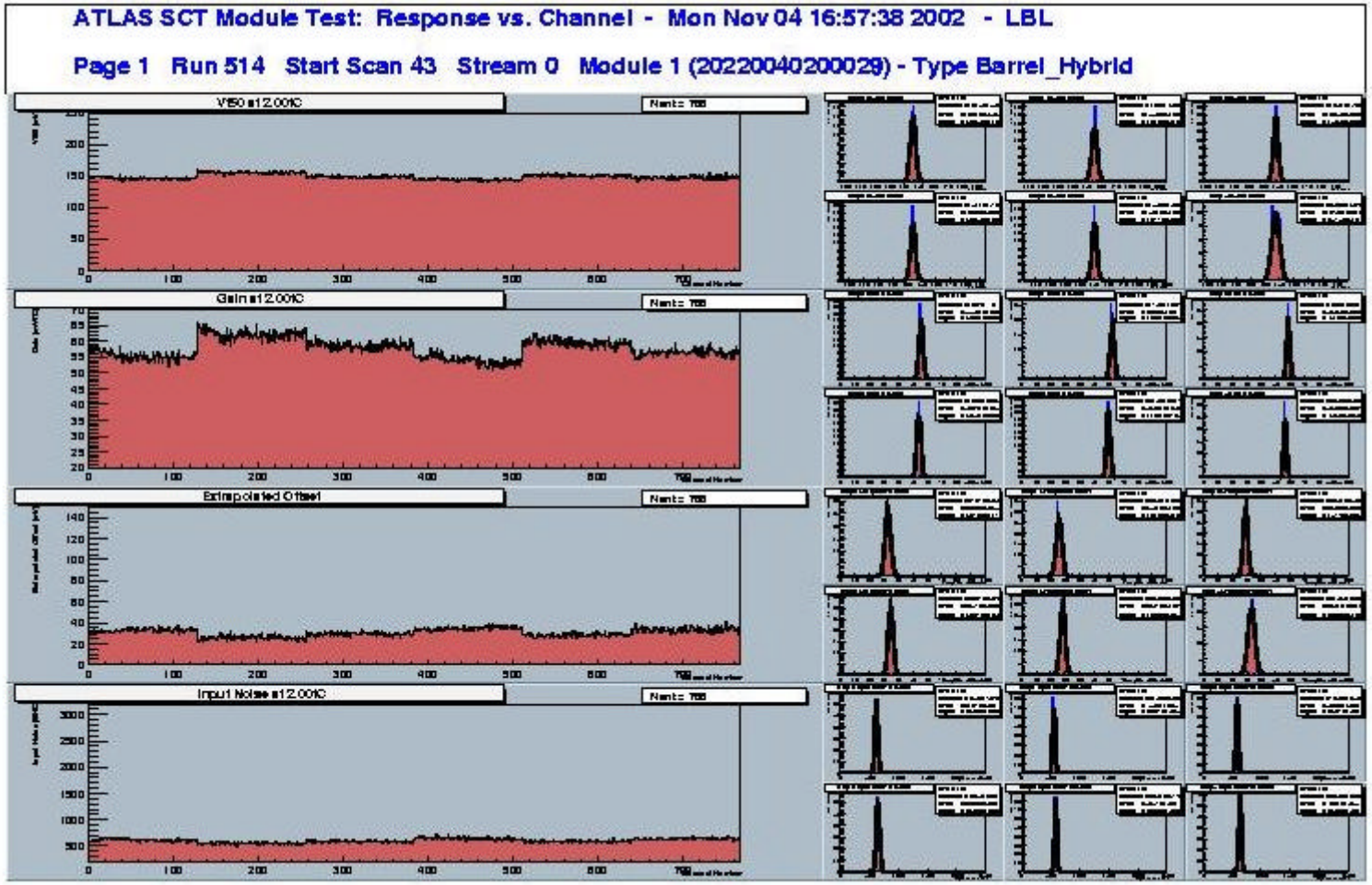
Large Gain Spread at cold 

Chip Response H29– Gain Spread at cold

Example of Gain Spread after trim at 0°C



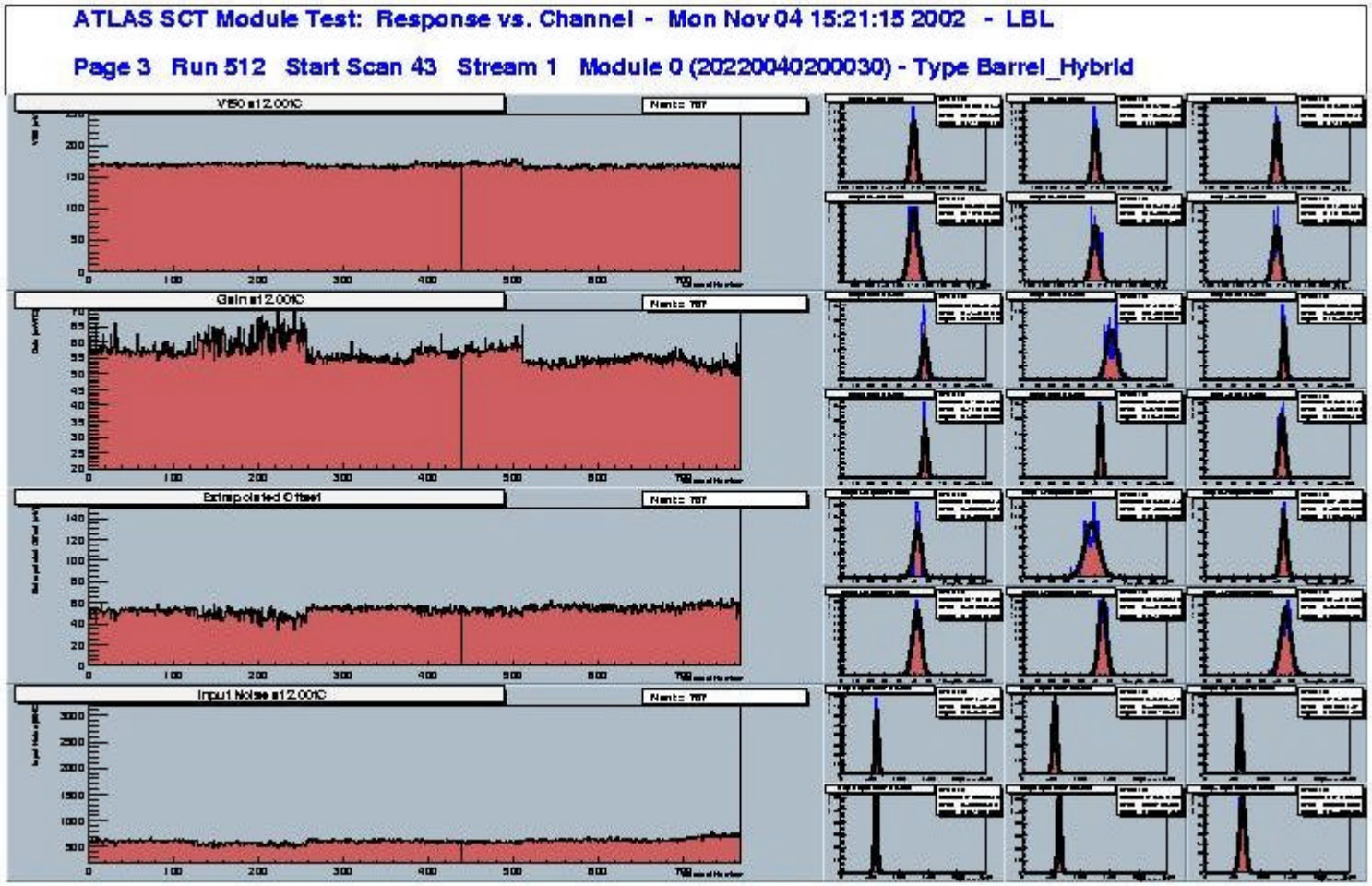
Chip Response H29– Gain Spread at cold – no 8fC point



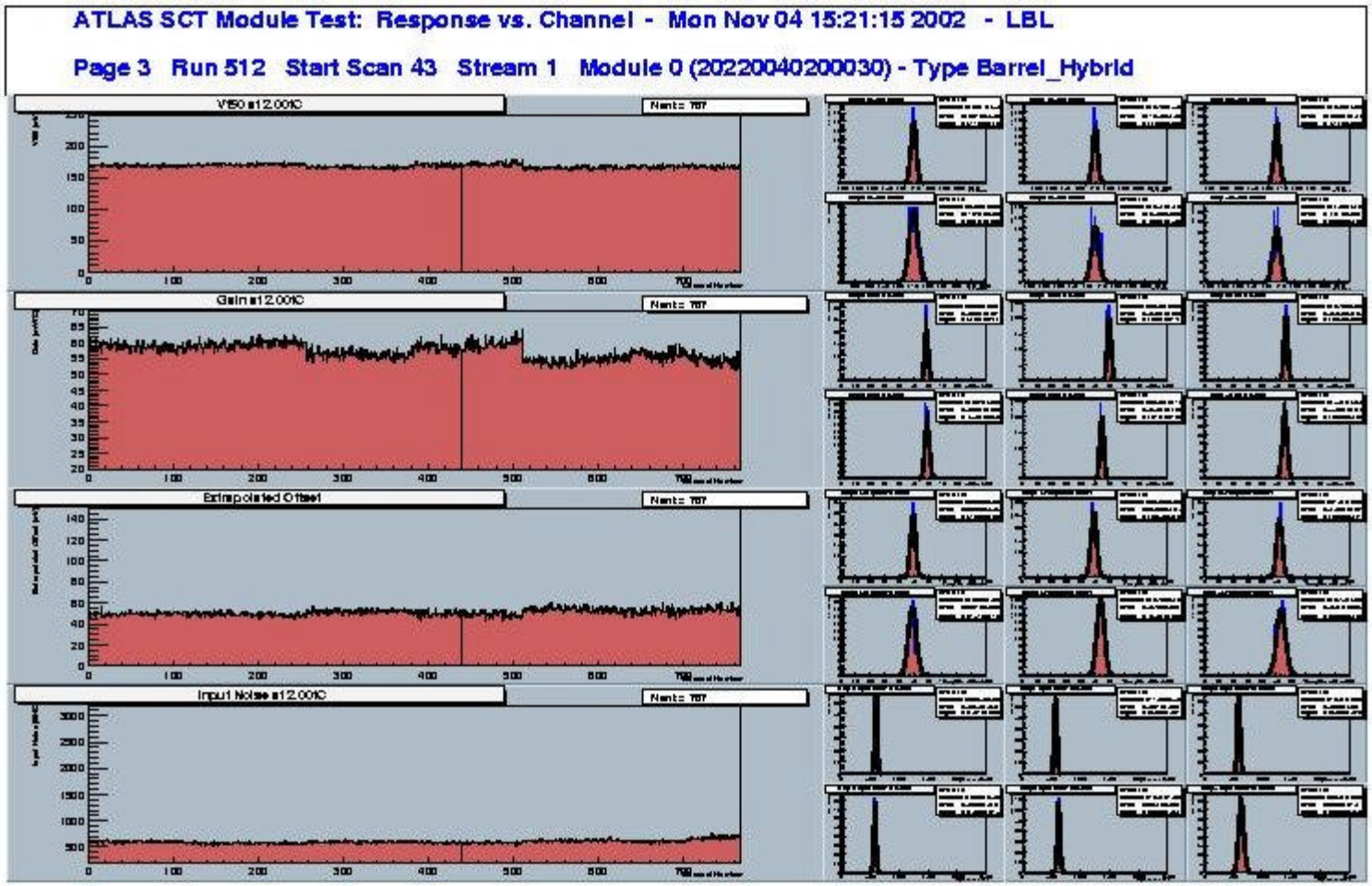
Same RUN but the fitting of the response curve excludes the last point (8fC)

Chip Response H30 – Gain Spread at cold

Example of Gain Spread after trim at 0°C



Chip Response H30 – Gain Spread at cold – no 8fC point



Same RUN but the fitting of the response curve excludes the last point (8fC)

Chip Response – New Cuts

- New cuts in the TrimRange Scan algorithm

- Noisy channels are now identified by the cut 1.15*(chip mean noise)

- Code to automatically exclude suspect data due to "8fC effect"
  The fitted range is adjusted to exclude points (charge > 5.0fC)
  for which the output noise is > 1.5*the mean output noise taken over all charges

- Channels with anomalous gain are now identified as follows:
  hi_gain channels have gain greater than (1.25 * mean_chip_gain)
  lo_gain channels have gain less than (0.75 * mean_chip_gain).
  This is in agreement with the gain cuts used during chip testing.

Testing Time 

Testing Sequence

	Operation	Description of tests	Time
Hybrid	**Initial Characterization**	**Digital tests + Response Curve + NO + TW**	1 h
	S-curves		10 min
	perl archive + web		15 min
	Hybrid cold LTT	10 h at 0°C with every 2 h Confirmation + Single Characterization at the end	10 h + 6 h + 3 h
	S-curves		10 min
	perl archive + web		15 min
	Hybrid warm LTT	90 h at 37°C with every 2 h Confirmation + Single Characterization at end	90 h + 6 h + 3 h
	S-curves		10 min
	perl archive + web		15 min
Fan-out	**Confirmation**	**Digital tests + Three Point Gain**	15 min
Module	**IV Scan**	Scan up to 500 V (LV off) at 15°C	1 h
	Characterization	**Digital tests + Response Curve + NO + TW**	1 h
	S-curves		10 min
	perl archive + web		15 min
	Thermal cycling	Cycles from -30°C to +40°C (LV off)	20 h + 0.5 h
	Metrology		?
	Module LTT	24 h at 0°C with every 2 h Confirmation + Single Characterization at the end	24 h + 6 h
	S-curves		10 min
	perl archive + web		15 min

Testing Rate

Hybrids

• Characterization		1 h/hybrid
• Burn-In 37ºC		90 h + 6 h Characterization + 3 h Chiller setting
• LTT 0ºC		10 h + 6 h Characterization + 3 h Chiller setting
	OR	*10 h at 37ºC* *10 h at 0ºC*
• **6 hybrids every**		**~120 h (5 days)**
	OR	*~ 30 h (2 days)*

Modules

• IV test	1 h/module
• Characterization	1 h/module
• Temperature Cycles (6 modules)	24 h
• LTT 0ºC (6 modules)	24 h + 6 h Characterization + temp setting time
• **6 modules**	**every 2.5 days**

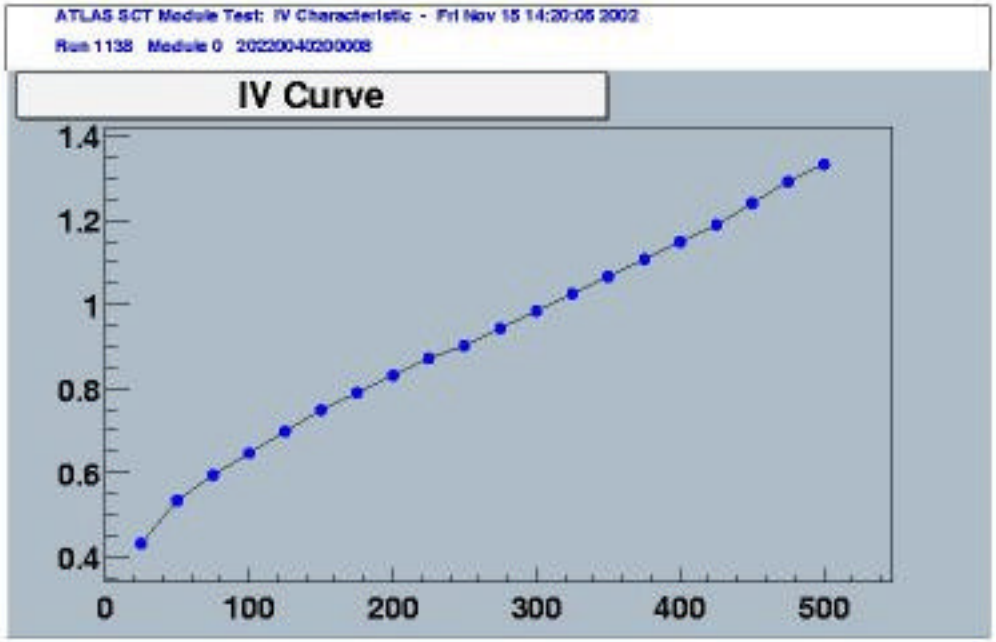
LTT-Burn-in Summary

- Overall a few channels and chips show higher noise (partbonded defects) or higher gain

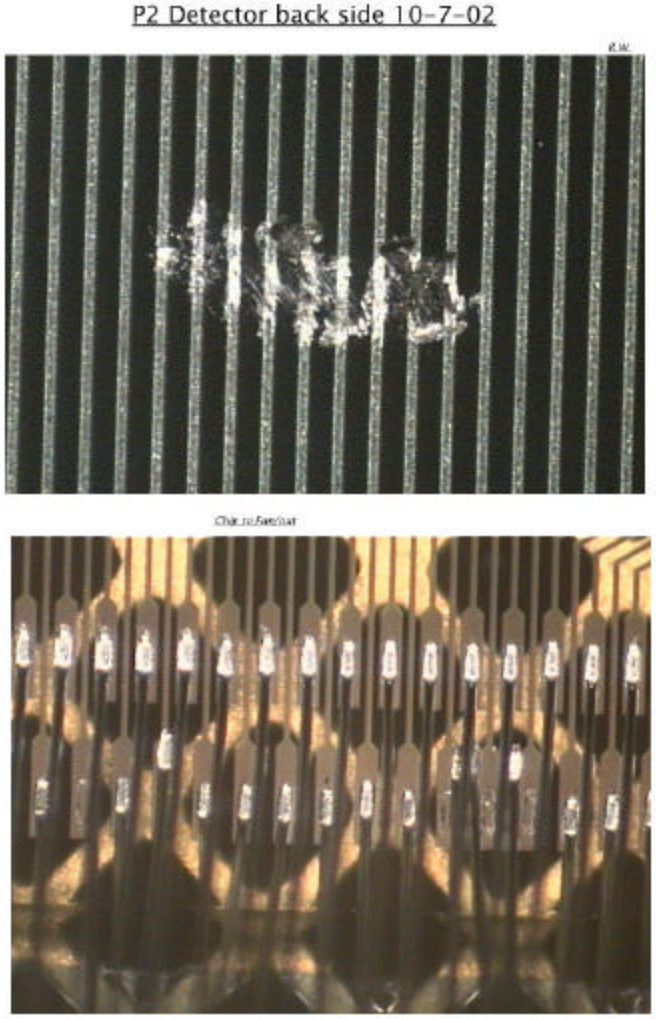
In particular:
202200402000010
687 high gain (15%)
202200402000013
All digital tests fail for chip 2-5 (but chip 2 seems to be responsible for the other ones)
202200402000010
1451 high gain (15%)
202200402000025
channel 941 has high noise during a single test
202200402000029
Chip 10 has 32 channels with higher noise (partbonded) and fluctuating

⟹ **All defects appear at the very first test**
we could reduce the duration of LTT

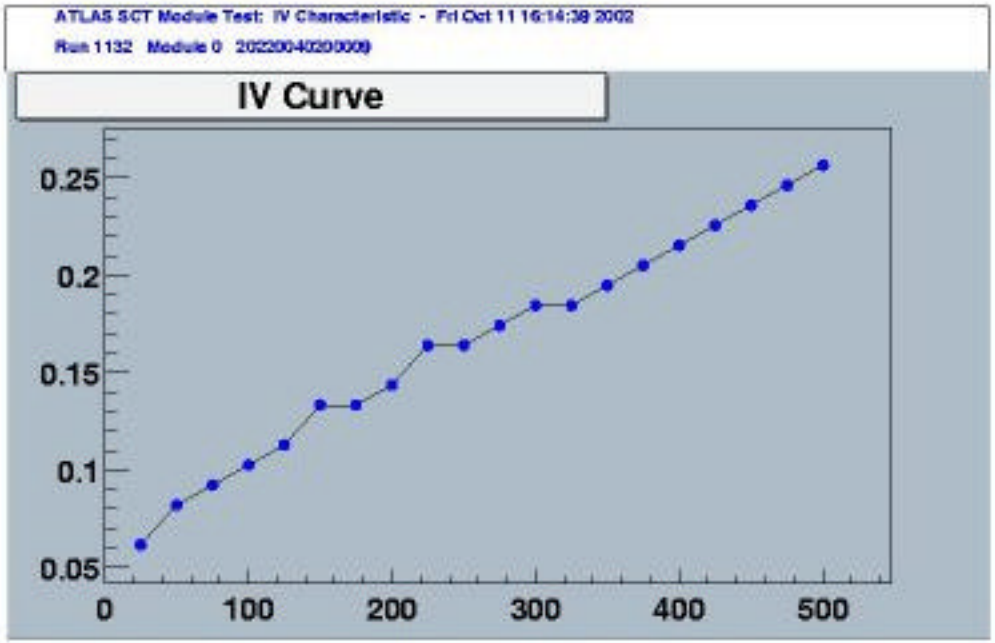
Modules 20220040200008



Noisy	Unbonded	Dead	Total
3	7	2	12



Modules 20220040200009

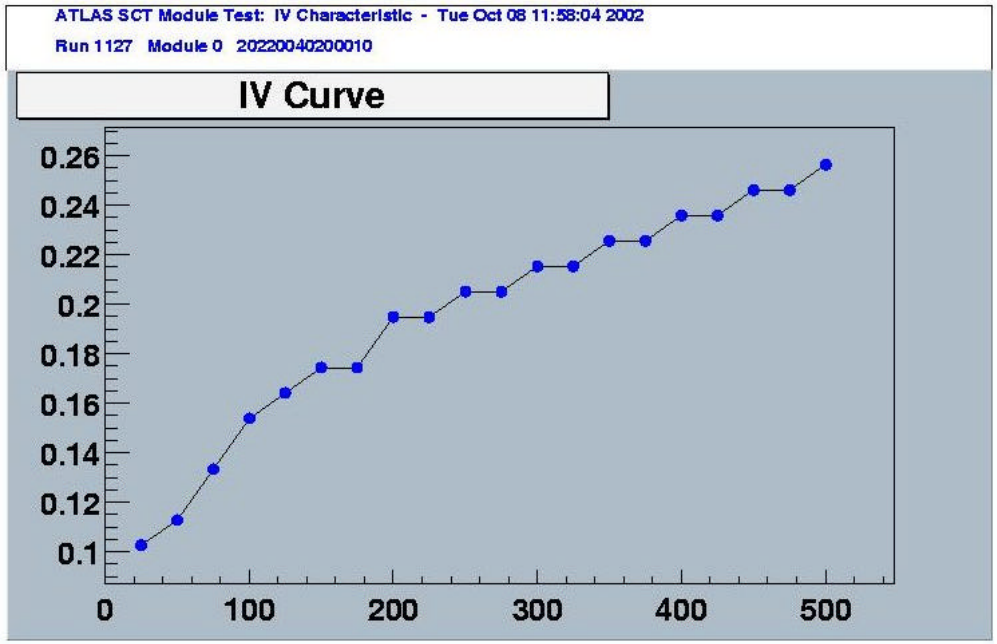


Noisy	Unbonded	Dead	Total
1	6	7	14

3 of the dead channels are because of a defect on the silicon

Modules 20220040200010

Noisy	Unbonded	Dead	Total
1	1	0	2



Summary

- Chip QA/Visual inspection show good yield but better care is required

- 2 (+2) chips replaced because defective after electrical testing
  Gain(2) Token(1) TW (1)

- Wafer/Hybrid comparison seems to be an effective tool for chip selection
  Chip replacement
  Chip selection before use

- First 29 hybrids my suffer from PA problem

- New features/cuts in the software will help with anomalous chip response

- Burn-in time could be reduced to 10 h
  All defects show up at the very first test