# Status of the ASIC Test System for SCT

Alessandra Ciocio
Lawrence Berkeley National Lab

- Overview
- Status of the Hardware
- Status of the Software
- In Progress and Next

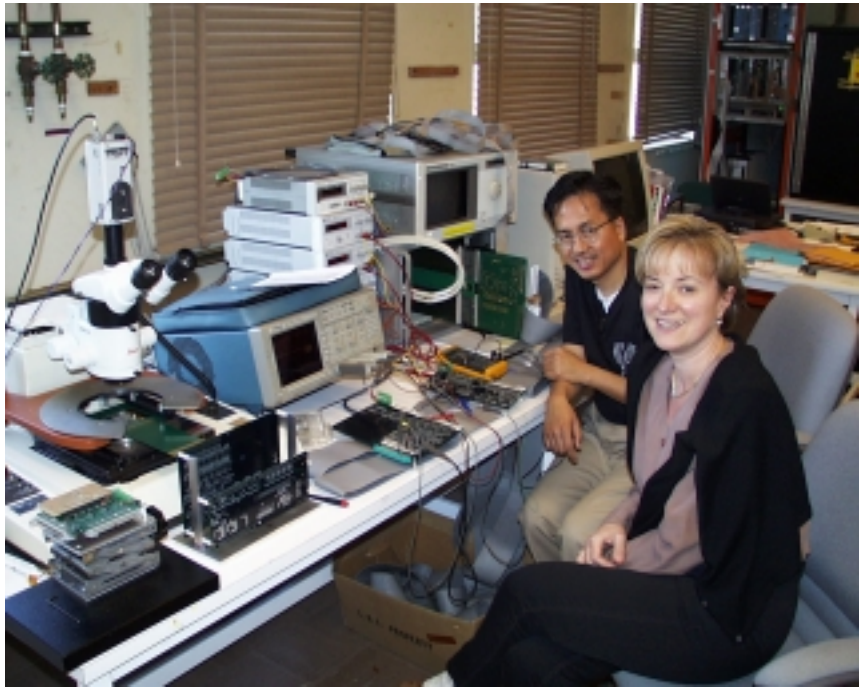
# Overview

Original LBNL design (Hubert Niggli)
Currently under debugging and production at LBNL by:

Alessandra Ciocio, Vitaliy Fadeyev,
Chinh Vu, Thorsten Stezelberger,
Rhonda Witharm

Gil Gilchriese, Carl Haber,
Francesco Zetti

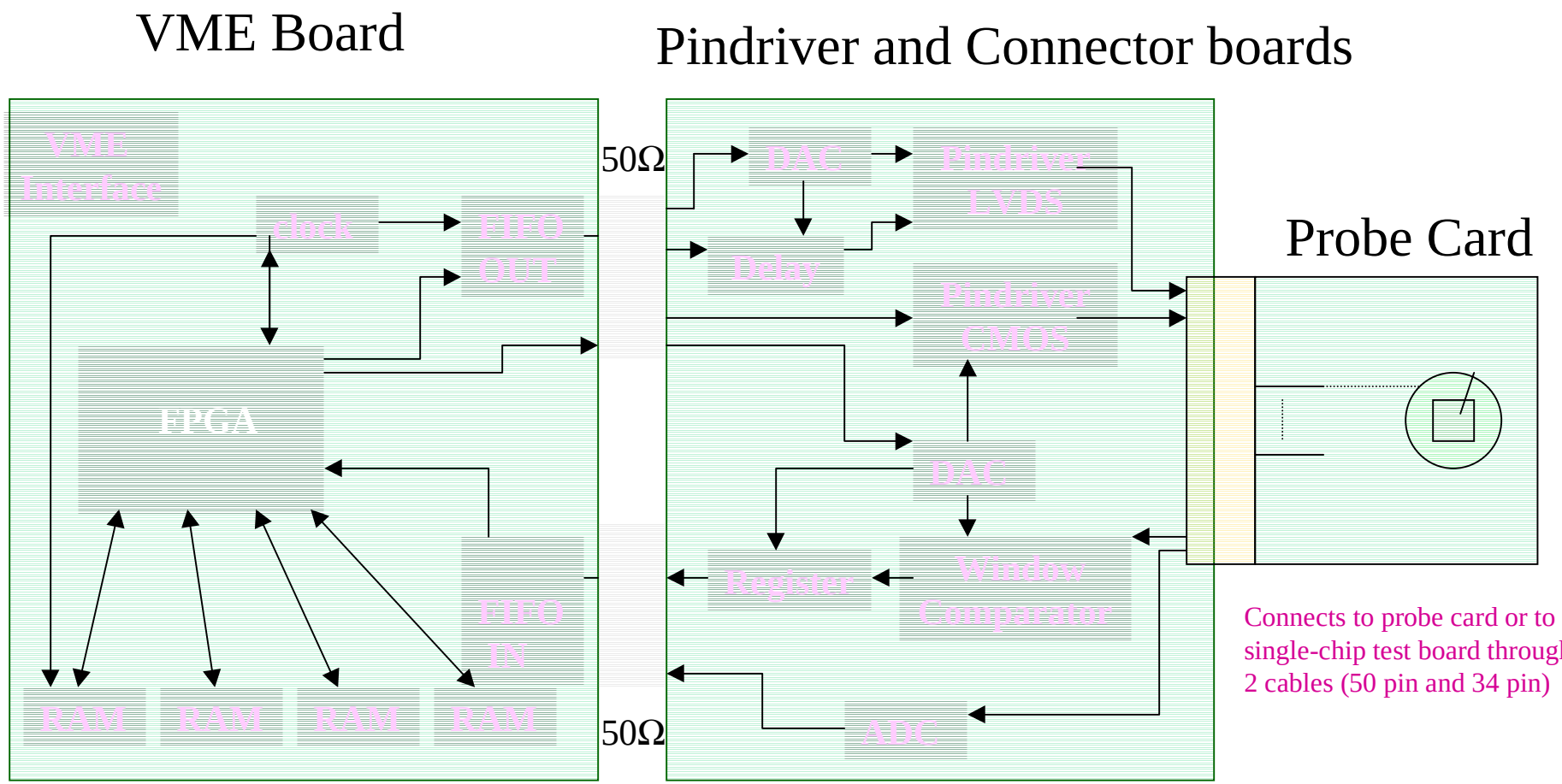
George Zizka, Helen Chen



*UC SantaCruz*
Alex Grillo, Abe Seiden,
Max Wilder, Ned Spencer

*CERN*
Francis Anghinolfi, Jan Kaplon, Wladek Dabrowski, Wojciech Bialas, Carlos Lacasta (Valencia)

# Overview




Connects to probe card or to a single-chip test board through 2 cables (50 pin and 34 pin)

All operations are programmed in the FPGA using VHDL
On-board comparison of chip response to testvectors with Verilog simulation. The simulation vector is stored in the sim vector memory. The result of the comparison is one bit in the FPGA status register. Frequency from 40-80 MHz

Allow to adjust amplitude and delays of the signals within a range to test functionality of ABCD by feeding them through pindriver and delay chips.
DACs allow to vary parameters.
Signals from ABCD go through window comparator.

# Status of the Hardware

## Major steps for the past six months

- **During the summer we went through submission of new layout for all boards:**
  **VME Board, Pindriver and Connector Boards**
  - **We kept the original design but we fixed major bugs**
  - A50 pin and a 34 pin 3M connectors replaced the 128 pins edge connector on Connector Board
  - **We assembled Pindriver and Connector Board in a box with a built-in fan for cooling**

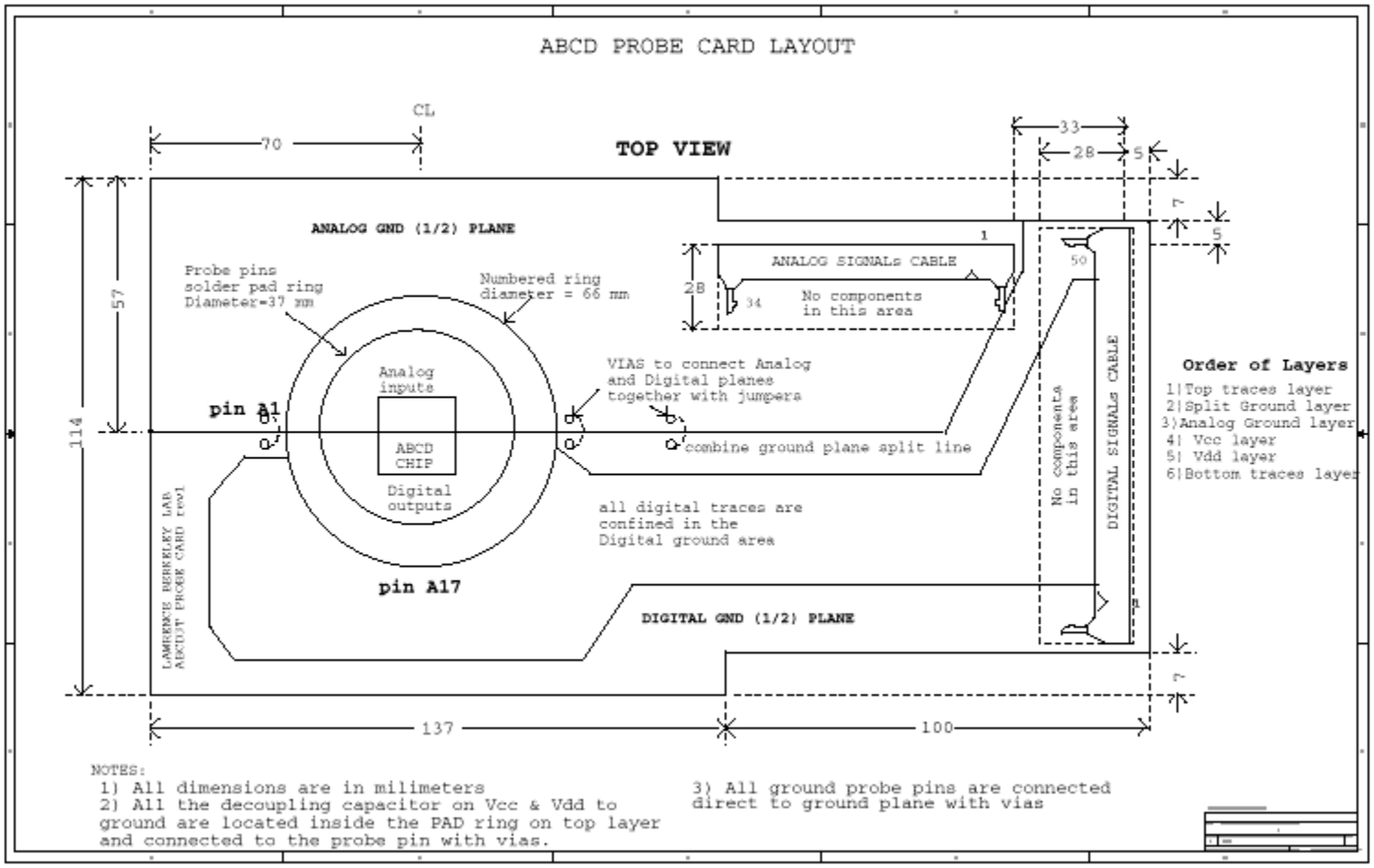
  **Probe Card**
  - **We designed a custom card to accommodate for different probe stations geometry**
    - Differential pair signals are layout in parallel and on the same trace layer
    - Low frequency filter is applied to the differential threshold lines (VT1, VT2) and Shaper+Preamp Current lines
    - 6 layers (50 ohm matched impedance ,full body gold ) in the following order:
      Top traces, VDD, Digital and Analog layer spit plane, Analog ground, VCC, Bottom traces layer

  **Single-chip test Board** (see slide)
- **We sent one of two prototype systems to Carlos Lacasta (Valencia) to start developing software (July)**
- **Vitaliy Fadeyev (postdoc) joined the LBNL group in July**
- **New system was available at LBNL in September**
- **We sent a new system to CERN (October)**

- **Vitaliy and Sandra (no Chinh) spent a week at CERN (November) to work with Carlos, Francis, Wojciech, and Jan, to debug software and implement digital test set (testvectors).**
  **Brought a system for RAL at CERN but discovered one faulty board (with Terry Pritchard)**

# Status of the Hardware

## Probe Card Layout




All the decoupling capacitors are located as close as possible to the probe pins

All resistors are located around 1” from the probe pins solder pads

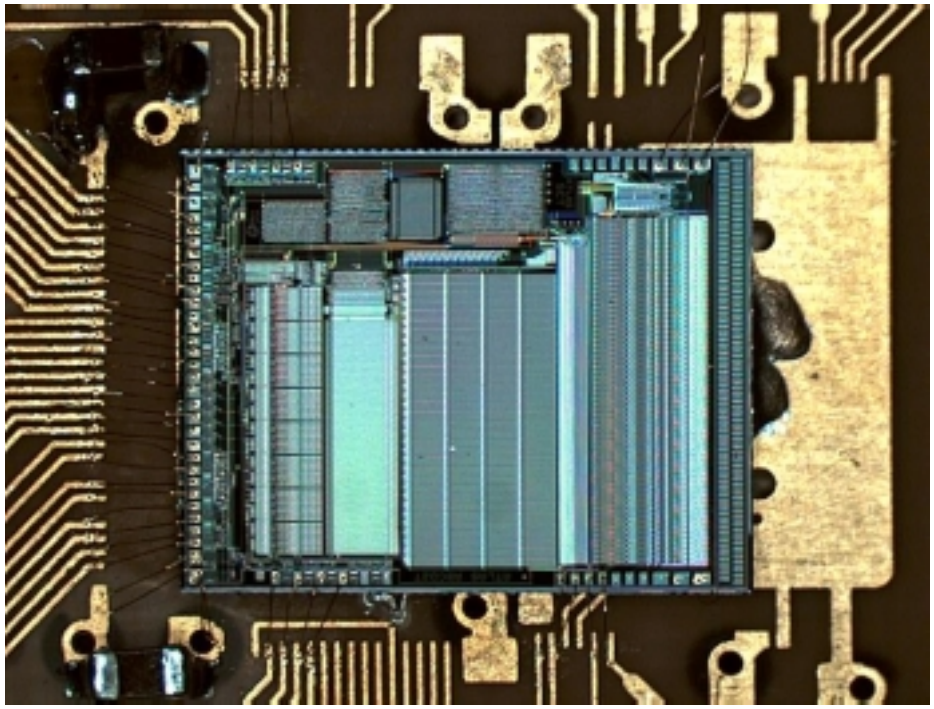
All inductors are located close to the connectors

A50 pin and a 34 pin 3M connectors replace the 128 pins edge connector

# Status of the Hardware

## Single-Chip Test Board


The single-chip test board is mounted on an adaptor card that redirect signals from its 64 pin connector to the 50 and 34 pin connectors as the ones on the probe card.
It allows to plug in the same cables that connect to the probe card directly



# Status of the Software

We have a stand-alone software to perform Threshold Scan and Testvectors at LBNL
running on PC/WNT, controlling VME using NI-MXI/PCI interface

- In mid-November the new system functionality have been merged into CERN screening software (Visual C++ application, running on PC/W95 developed by Carlos) and Analogue + Digital tests except 2 tests have been implemented (Verilog simulation is provided by Francis)

  the full implementation was not completed due to the failure of the comparison between the chip response and the Verilog simulation Now working!

- We need to define the additional tests that the new system allows like phase and signals amplitude margins for a better characterization of the IC's
  and to agree on the final test specification list to satisfy Temic requirements for guaranteed yield and possible upgrade with the additional tests of the Test Specification for Wafer Screening document

- Documentation in progress

# In Progress and Next

- **The debugging of more boards at LBNL is in progress:**

**VME Board:** Fixed the clock distribution circuitry by making the synthesizer clock working for both testvectors and threshold scan (to avoid manual switching between general 40 MHz clock and synthesizer with variable frequency)

**Pindriver Board:** Until recently the 2 Threshold and Shaper + Preamp Current lines were disconnected at the probe card (and single-chip test card had no bonds corresponding to those pads) because they introduce excess noise in the analogue measurements. This problem has been solved with a fix on this board and now we have a complete reading of the ADC

**Probe Card:** Low frequency filter has been applied to the differential threshold lines (VT1, VT2) and Shaper+Preamp Current lines. Analogue measurements (threshold scan) with probe card show higher noise than with single-chip test card but still of an acceptable level (~8 mV R.M.S.)

New boards will be produced or list of fixes to apply on existing boards will be documented

- **The debugging of the VHDL code for the last few remaining problems is in progress:**

  - Testvectors comparison (now working as a few days ago)
  - Identification of Testvectors location of difference/failure

- The wafer screening software will be completed with all standard digital test and additional tests as soon as we will have a fully operational system

- A full comparison of the CERN and the LBNL systems will be performed first by testing the wafer from the second batch (#11) at LBNL and comparing with the results with the ones that Jan provided from wafer screening performed at CERN

- Mid-January possible return of LBNL crew to CERN for verification of new system