An Analog Front-End Bipolar-Transistor Integrated Circuit for the SDC Silicon Tracker

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Abstract

A low-noise, low-power, high-bandwidth, radiation hard, silicon bipolar-transistor full-custom integrated circuit (IC) containing 64 channels of analog signal processing has been developed for the SDC silicon tracker. The IC was designed and tested at LBL and was fabricated using AT&T's CBIC-U2, 4 GHz f_T complementary bipolar technology. Each channel contains the following functions: low-noise preamplification, pulse shaping and threshold discrimination. This is the first iteration of the production analog IC for the SDC silicon tracker.

The IC is laid out to directly match the 50 µm pitch double-sided silicon strip detector. The chip measures 6.8 mm x 3.1 mm and contains 3,600 transistors. Three stages of amplification provide 180 mV/fC of gain with a 35 nsec peaking time at the comparator input. For a 14 pF detector capacitance, the equivalent noise charge is 1300 el. rms at a power consumption of 1 mW/channel from a single 3.5 V supply. With the discriminator threshold set to 4 times the noise level, a 16 nsec time-walk for 1.25 to 10 fC signals is achieved using a time-walk compensation network. Irradiation tests at TRIUMF to a $\Phi=10^{14}$ protons/cm^2 have been performed on the IC, demonstrating the radiation hardness of the complementary bipolar process.

I. INTRODUCTION

Since 1989 the Solenoidal Detector Collaboration (SDC) has been developing a general purpose detector to be operated at the Superconducting Super Collider (SSC). A technical design report was presented on April 1992 [1]. The baseline tracking system is composed of an inner silicon and an outer straw-tube tracker. The silicon tracker, which consists of approximately 17 m^2 of instrumented silicon strip detectors with over 6 million electronics channels, provides precision vertex and momentum measurement and is also the key instrument for pattern recognition in the overall detector [2].

The silicon tracker is composed of a barrel region consisting of concentric cylindrical layers of double-sided silicon strip detectors, which provide axial and small-angle stereo measurements. Double-sided disk detector arrays on each end of the barrel complete the system. Each double-sided detector is 300 µm thick and has a strip pitch of 50 µm. Choice of a stereo angle of 10 mrad reduces "ghosts" at high track densities and also allows placement of all readout ICs at the same edge of the detector without use of additional signal routing. A strip length of 12 cm was chosen to minimize the number of readout ICs and associated material in the readout hybrid. Detailed studies showed that this is the maximum strip length that allows the required performance specifications to be met throughout the design lifetime of the detector [3]. The 12 cm long modules are formed by wire bonding two 6 cm detectors end to end.

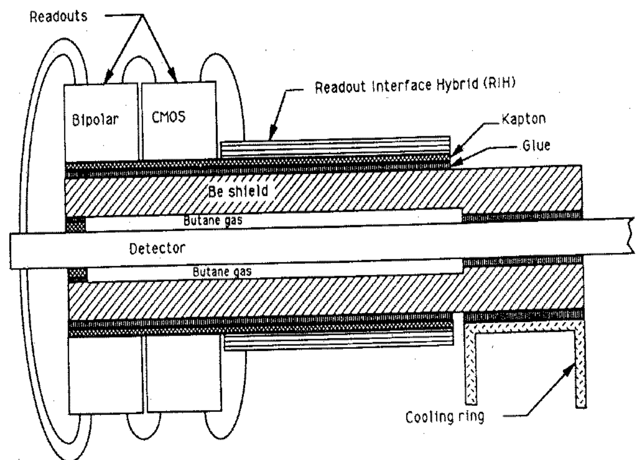

Figure 1. Cross section through a detector module.

A prime goal in the tracker design was to find the simplest system that would meet the physics goals of the collaboration. Detailed simulations of event reconstruction and detector response have shown that a digital readout, i.e. readout of hit information alone without analog information, is quite adequate. The front-end electronics chain is subdivided into two separate ICs. Low-noise preamplification, pulse shaping, and threshold discrimination are provided by an analog bipolar-transistor chip, while time stamping, data buffering and sparse readout are provided by a digital CMOS data storage chip. This combination yields the lowest overall power with a small penalty in total chip area. The detector and the two ICs are bonded together to form the full front-end detector module. The baseline design utilizes a polyimide-based hybrid for the electronic readout module. This assembly (including an intermediate Be shield and insulator sandwich) is mounted directly on the detector with a minimum of additional mass (Figure 1).

This paper reports the design and test results of a low-noise, low-power, high-bandwidth, radiation hard, first

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Strip length	12	cm
Strip pitch	50	μm
Metal resistance	50	Ω/cm
Strip capacitance	1.2	pF/cm
Coupling capacitance	12	pF/cm
Bias resistor	200	kΩ
Leakage current ($T=0^oC$. $\Phi=10^{14}$ cm^{-2})	100	nA/cm

Table 1: Double-sided silicon strip detector.

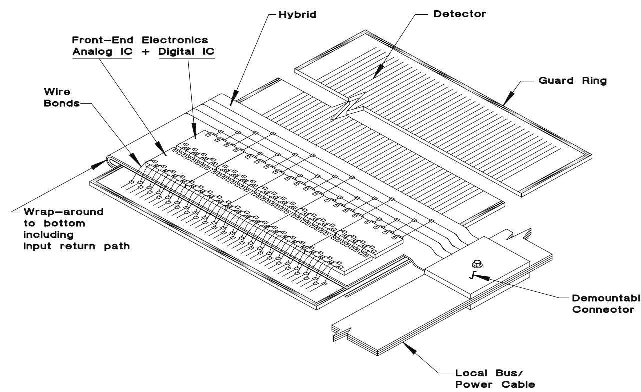


Figure 2. Conceptual layout of detector module.

prototype 64-channel analog signal processor IC for the SDC silicon tracker. Although intended primarily as a proof of principle and a vehicle for detailed system test, this IC was designed as a fully-qualified readout device that already is quite suitable for use in a detector system.

II. SYSTEM REQUIREMENTS

The basic system requirements of the analog front-end electronics are reviewed briefly in this section. A detailed discussion has been presented by Spieler [4]. Design parameters for the front-end circuitry are driven by a few primary performance criteria:

1. Efficiency > 99%;
2. Operational lifetime > 10 years at the design luminosity of 10^{33} cm^{-2} s^{-1};
3. Power dissipation ≤ 1 mW per analog channel.

These requirements translate to the following electronic design parameters, which need to be maintained throughout the operational lifetime of the detector, i.e., up to a fluence of 10^{14} cm^{-2} and an ionizing dose of 3.5 Mrad (Si).

1. Equivalent noise charge $Q_n \leq 1400$ el. rms (C_s=15 pF);
2. Comparator threshold $Q_t \geq 4Q_n$;
3. Time resolution < 12 ns ($1.25 \leq Q_s \leq 10$ fC);
4. Double-pulse resolution ≤ 66ns (successive 4 fC signals).

The design is specified to include at the outset all parasitic contributions and parameter changes anticipated until the end of the operational lifetime. System performance would initially be superior to design specifications, and gradually degrade with time.

The detector strips are ac coupled to the electronics and have the characteristics listed in Table 1. Each detector contains 640 strips per side (Figure 2). To connect all strips, the electronic pitch has to be < 50 μm to compensate for the dead space at the chip periphery and between ICs. To minimize this dead space, bias and control signals are bussed across the IC, with pads on opposite sides, to allow direct chip-to-chip interconnection rather than chip to substrate. This arrangement also simplifies trace routing on the readout hybrid, with a reduction in area and material.

Since the silicon tracker has several million channels of electronics, reliable control of cross-talk and any other causes of spurious hits is of extreme importance. Data and control signals to and from the module use differential lines to reduce cross-coupling. In addition to providing noise immunity differential lines are essential for the control signals (especially the threshold lines) to minimize the effect of voltage drops. Signal transmission in the front-end chain between the analog and digital ICs is either by differential lines or by a localized loop that allows separation of the analog and digital grounds.

Thresholds are externally adjustable to accommodate differences in signals between the n- and p-side of the detector and to adapt to increases in noise with radiation damage. Good threshold control is critical, so the absolute value of the threshold voltage should be high to mitigate transistor mismatch over a die and within a module, and to provide adequate system noise margin. A minimum differential threshold voltage of 100 mV, corresponding to a 1 fC nominal threshold, was selected. This requirement sets the minimum gain of the amplifier chain equal to 100 mV/fC. In the interest of reducing material and cost per channel, a minimum die area was targeted.

III. INTEGRATED CIRCUIT DESIGN

A. Technology

After a careful comparison of the obtainable performance within the required power consumption with available radiation hard CMOS technologies [4], a bipolar-transistor front-end IC was selected to realize the analog signal processing. Three vendors with commercial bipolar processes that meet SSC/LHC radiation hardness, speed, and layout density requirements have been identified. None of these processes were explicitly developed for a high-radiation environment, but are inherently radiation resistant. AT&T Microelectronics' CBIC-U2 complementary bipolar process was chosen for the first prototype IC, in spite of having a marginal speed performance, because at the time the design was started the radiation resistance of its npn and pnp transistors had been proven [5, 6] and AT&T's technical support greatly facilitated the design. Since this first prototype circuit was meant as a proof of principle for the silicon tracker front-end electronics, we accepted inferior double-pulse and

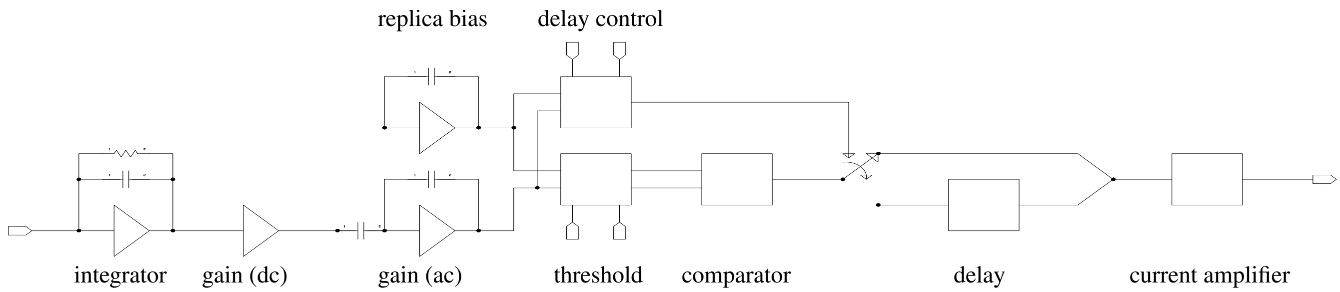


Figure 3. Single channel block diagram.

time resolution and a larger die size than targeted for the production chip. A second iteration design is underway that will meet all the design requirements by utilizing AT&T's new CBIC-V2 process, which exhibits higher speed and denser geometry than the U2 process. Transistors in the V2 process have been irradiated to a fluence of Φ=1.2x10^{14} cm^{-2} (800 MeV protons at LAMPF) and still exhibit adequate performance [4].

The CBIC-U2 complementary bipolar junction isolated process features 4.5 GHz vertical npn and 3.75 GHz vertical pnp transistors. Minimum size npn and pnp transistors have areas of 32 x 50 μm^2 and 40 x 55 μm^2, respectively. The process supports two types of diffused resistors with sheet resistances of 50 Ω/❐ and 1080 Ω/❐. Two types of capacitors are available: metal-nitride-oxide-silicon (MNOS) and metal-on-metal (MOM), with MNOS capacitors being used for values greater than 0.75 pF. CBIC-U2 has first and second level titanium-platinum-gold metallization with 5 μm and 7 μm pitch respectively.

B. Architecture

A data driven, fully asynchronous architecture is used. The front-end circuitry requires no external clocking to acquire signals and become ready for the next hit. Continuous shaping integrates the signal current and returns to baseline automatically. If the signal exceeds a selectable threshold, the time of occurrence is recorded (in bins corresponding to beam crossings) and stored until receipt of a level 1 trigger accept. Each channel on the analog IC contains the following functions:

1. Charge integration;
2. Pulse shaping;
3. Threshold/timing discrimination.

Figure 3 shows a single channel block diagram. The first stage is a low-noise charge-sensitive preamplifier, which integrates the current pulse delivered by the silicon strip detector. The voltage signal at the output of the integrator is then amplified and further filtered by a dc-coupled gain stage followed by an ac-coupled amplifier. The third stage is ac coupled since the high gain provided by the three cascaded stages would result in excessive dc base line shift at the comparator input. After the third stage the signal path becomes fully differential. The second input of the differential amplifier is biased from a dummy amplifier that is a replica of the ac amplifier. The biasing stage is included in each channel to minimize channel-to-channel variations.

Due to the marginal gain-bandwidth product obtainable with the CBIC-U2 process within the required power dissipation, the shaping time of the amplifier chain was set to about 35 ns instead of the 20 ns as would be optimum from the detector collection times [7]. The integration time is determined by the cumulative upper 3-dB frequencies of the cascade of stages, with all stages exhibiting similar bandwidth, i.e., no stage contributing a dominant pole. The differentiation time is determined by the resistive discharge of the feedback capacitor in the integrator and by the low frequency roll-off of the ac gain stage.

Besides defining the threshold, the comparator also serves as a simple leading-edge timing discriminator. As such, a major problem in achieving the required time resolution is time-walk with amplitude variations, that is, for a fixed threshold and constant peaking time, signals with higher peak amplitudes will cross the threshold earlier than smaller signals. Most of the time shift occurs at small overdrives. To maintain single-bunch resolution a simple walk compensation circuit was included. This network utilizes a second comparator to insert an additional delay for larger signals. The signal threshold at which the delay is switched in is set by a separate differential delay control signal, similar to the threshold control. Ideally, this delay is 1/2 of the total time-walk, so that the output timing folds back to yield a total time-walk that is half of the uncompensated circuit. The detailed nature of the walk vs. amplitude is not important, as long as all output pulses resulting from signals in the 1.25 to 10 fC range fall within one time bucket. Although other circuits can provide near perfect time-walk compensation, they require either more power or area than this simple scheme.

The comparator output is amplified and fed to the digital IC as a current signal. The goal is to maintain a high impedance between the power supplies feeding the two ICs, so that analog and digital power and ground can be isolated to avoid coupling.

The severe limitations on power consumption and space dictated a design philosophy of simplicity. Many of the circuit functions could have been done with more elegant and/or higher performance topologies, but device count and current were the highest priority. The IC operates from a single 3.5 V supply at a 1 mW/channel power consumption.

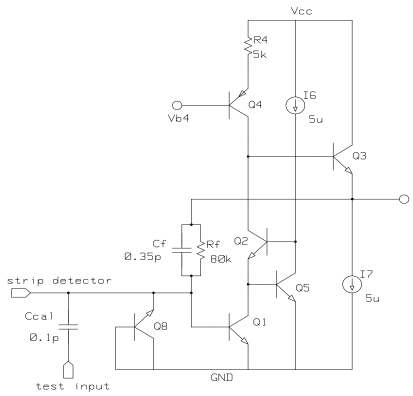


Figure 4. Integrator schematic.

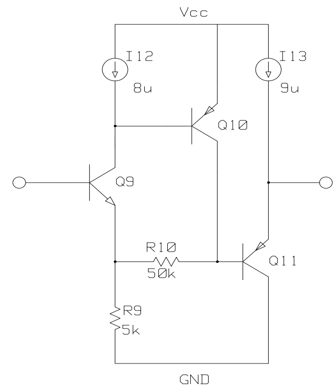


Figure 5. dc amplifier schematic.

C. Circuit Blocks

The integrator is configured as a single-stage common-emitter cascode amplifier (Figure 4) with an active load and an RC network in the feedback loop. The most critical parameter in the charge-sensitive preamplifier is the bias current in the input device Q_1, which determines the speed and noise. For a shaping time of τ=35 ns and a strip capacitance of C_s=15 pF, a nominal input transistor current of 140 µA is needed for minimum noise. To preserve full control of this parameter, I_{Q1} is set externally through a low-noise current mirror (Q_4 and R_4) common to all channels on a chip. The size of Q_1 is determined as a compromise between base resistance (r_b), junction capacitance (C_j), and common-emitter dc current gain (β) characteristics after irradiation. In principle, a large input device would be desirable to reduce the noise contribution of the base resistance. On the other hand, as the volume of the base-emitter junction increases, the effect of radiation damage on β becomes more pronounced, so that a small device with peak current gain at I_c=140 µA is preferable. An input device with r_b=45 Ω, C_j=0.8 pF, and with better radiation tolerance at the nominal bias, was selected. Values for C_f and R_f are the result of extensive SPICE simulations, including on- and off-chip parasitics as well as process variations, with the objective of maximizing the gain while preserving adequate stability and speed of response. An "active cascode" circuit (formed by Q_2, Q_5 and I_6) is used to reduce the cross-coupling through the common line at the base of Q_2 that a regular cascode would require. Diode Q_8 is added for input protection, and a 100 fF calibration/test capacitor is included at the input of each channel. With the nominal strip capacitance of 15 pF, the integrator has a gain of 2 mV/fC with a peaking time of 20 ns and a peaking frequency of 11 MHz. The mid-band equivalent input noise voltage and current spectral density are 1.7 nV/√Hz and 0.7 pA/√Hz respectively. The preamplifier consumes 525 µW, approximately one half of the total power budget.

The dc amplifier (Figure 5) is configured as a two-stage series-shunt feedback circuit. The voltage gain is approximately given by $(1+R_{10}/R_9)$. The series-shunt feedback provides broad band gain and a high input impedance, necessary to avoid loading the integrator. The amplifier has a voltage gain of 20 dB with f_{-3dB}=12 MHz at a power dissipation of 110 µW. As mentioned above, ac coupling to the following stage is necessary to allow for potential large excursions in the quiescent voltage at the output, caused by process variations or change in β during irradiation.

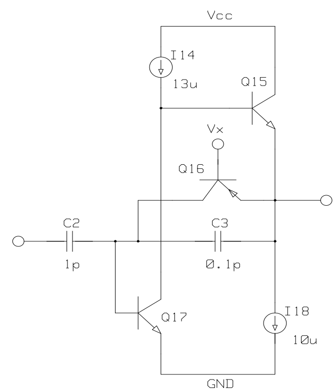


Figure 6. ac amplifier schematic.

The ac amplifier is a single-stage common-emitter circuit (Figure 6) with shunt feedback connected as a simple inverter amplifier with a voltage gain of C_2/C_3. V_x is generated on-chip and is common to all channels. To provide a monotonic return to baseline of the signal pulse, a single differentiation in the overall transfer function (the one provided by the integrator) would have been preferred. However the ac stage produces a second differentiation that is in practice limited by the base current and the values of capacitance and resistance available, and whose time constant is of the same order of magnitude as the integrator's. This time constant is adjusted to provide adequate baseline recovery of the signal pulse, as a compromise between excessive ringing and a slow return to baseline of the undershoot. The ac amplifier provides a gain of 4 to the shaped signal (equivalent to a voltage gain of approximately 20 dB at a peaking frequency of 10 MHz) with an 80 µW power consumption. The ac amplifier response is limited to unipolar signals. Figure 6 shows the schematic of the amplifier for the chip that connects to the n-strips in the detector, the output of the stage having a negative voltage swing. For the chip that connects to the p-strips, the ac amplifier is the dual of the one shown in Figure 6, i.e., pnp common-emitter with npn feedback transistor.

The replica bias circuit has the same configuration as the

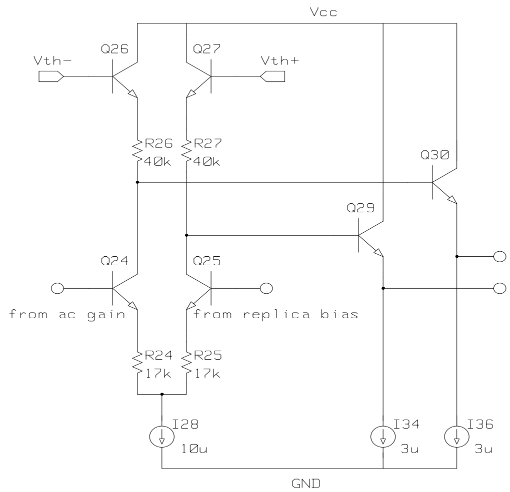
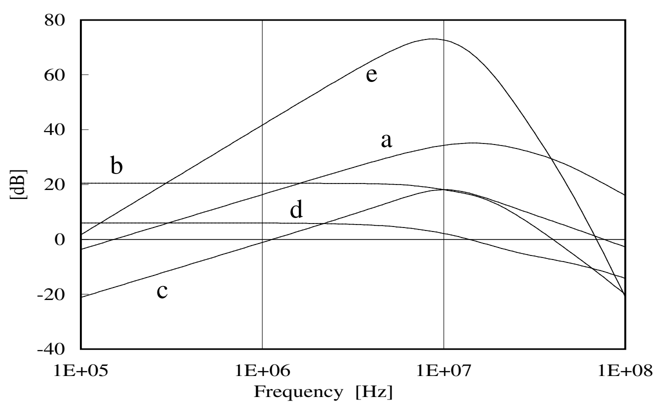


Figure 7. Threshold schematic.



(a) integrator, (b) dc gain, (c) ac gain, (d) threshold, (e) overall

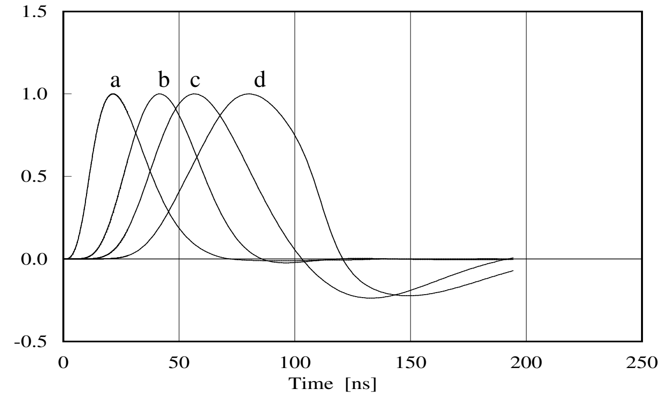
Figure 8. Simulated small signal voltage gain.

ac amplifier, to provide the exact same quiescent voltage at the second input of the differential circuit in the threshold and delay control blocks.

The threshold block (Figure 7) is configured as a simple differential amplifier with a voltage gain approximately given by R_{26}/R_{24}. The gain is set to a low value (~ 2) to reduce the contribution of the transistor's offset on the effective threshold uniformity. Transistors Q_{26} and Q_{27} present the differential threshold, given by (V_{th+}-V_{th-}), to the input of the comparator. The threshold circuit has an f_{-3dB}=9 MHz at a power dissipation of 55 µW.

The delay control block has the same configuration and characteristics as the threshold circuit.

The differential output of the threshold circuit is the end of the amplifier/shaper cascade. Figure 8 shows the simulated small signal voltage gain response in dB vs. frequency for each of the stages and for the overall transfer function with a 15 pF capacitor at the input. As mentioned above, all stages exhibit similar bandwidth with no stage contributing a dominant pole. The overall transfer function has a peak voltage gain of 4500 at ~10 MHz. Figure 9 shows the normalized voltage waveforms at the output of each stage. The input charge waveform used in the simulations is a realistic approximation of the signal



(a) integrator, (b) dc gain, (c) ac gain, (d) threshold

Figure 9. Simulated normalized voltage waveforms.

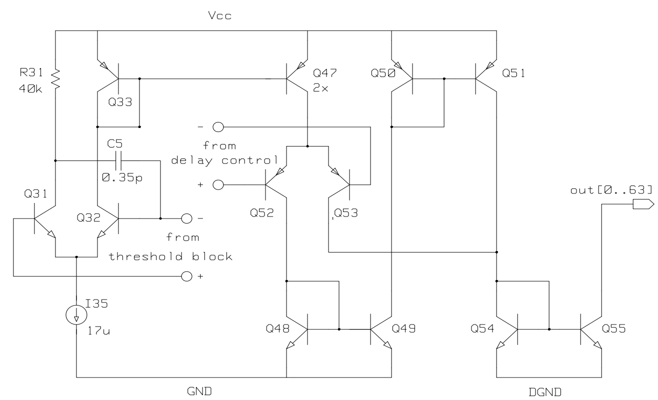


Figure 10. Comparator, delay and output circuit schematics.

delivered by the p-strips of the detector, with a collection time of 25 ns. The cascade of amplifiers delivers a shaped signal with an overall gain of 170 mV/fC.

Figure 10 shows the schematic of the comparator, the delay circuit and the output amplifier. The comparator consists of a simple differential pair (Q_{31} and Q_{32}) with ac positive feedback producing a regenerative circuit (Schmitt trigger). The major advantage of the regenerative comparator is the inherent self-latching action of the hysteresis loop. The circuit has a built-in noise immunity for a time interval defined by the RC time constant of the hysteresis loop. Once the comparator registers a hit, small perturbations will not cause re-switching. The price to pay is the broadening of the input pulse by the hysteresis time. As a compromise between noise immunity and pulse broadening a time interval of 14 ns was selected. Under quiescent operation the differential threshold voltage appears across the bases of Q_{31} and Q_{32}, keeping Q_{32} off. When a hit signal is generated, Q_{32} turns on, with its collector current going from approximately 2 to 17 µA. The current is mirrored and amplified (current gain of 2) by Q_{33} and Q_{47}. In the quiescent state the differential delay control voltage is applied across the bases of Q_{52} and Q_{53}, keeping Q_{53} on. For small signals, the output current from the comparator goes through Q_{53} directly into the output mirror, Q_{54} and Q_{55}. For large signals, Q_{53} is turned off and the output current from the comparator is routed through the mirrors Q_{48} - Q_{51}, delaying

Figure 11. Microphotograph of the 64-channel IC

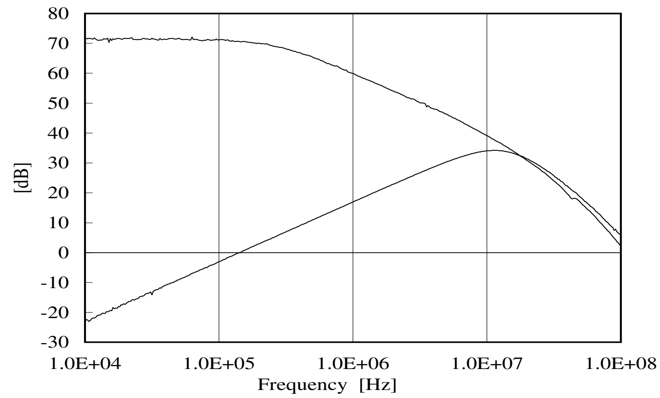


Figure 12. Measured integrator open and closed loop gain.

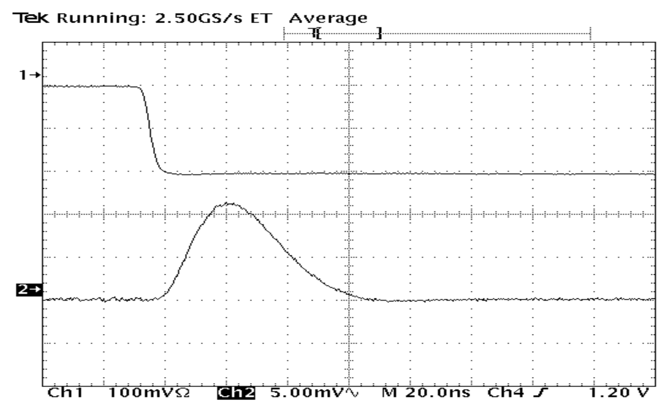


Figure 13. Measured integrator pulse response. Q_s=5 fC. The horizontal scale is 20 ns/division.

the channel output signal. The differential delay control voltage (V_{d+}-V_{d-}) defines the signal amplitude at which the delay element is inserted. For intermediate signal levels, the output current waveform will exhibit some non-linear switching characteristic. As mentioned above, the detailed nature of the output waveform is not important, as long as the trigger points of the time stamp for signals in the 1.25 fC to 10 fC range fall within one time bucket. This simple delay circuitry has the beauty of using only a few transistors and having no quiescent power dissipation. The comparator dissipates 87 µW, bringing the power consumption of the complete channel to 1mW.

The output stage is an open collector transistor (Q_{55}) that satisfies the requirement for a high output impedance. The basic principle is to ensure that all connections between the digital and analog ICs present a high impedance to current spikes originating in the digital circuitry so that interference does not propagate through the input signal path.

The output signal is a current pulse with a peak amplitude of 35 µA. This low level signal is adequate because it drives a receiver on the digital chip that is only a bond wire away, with a minimum of node parasitics. To comply with the design philosophy of localized loops - in order to separate analog and digital grounds - the emitters of Q_{55} on all channels are tied to a separate ground on the chip, which would then be wire bonded to the ground on the digital IC. The transistors (Q_{51}, Q_{53}) which drive the output current mirror have a high output impedance to provide noise immunity from the digital ground.

D. Layout

The electronic channel was laid out on a 40 µm pitch so that the chip width allows direct bonding to the 50 µm pitch detector strips as explained above. Given that 40 µm is the minimum dimension of the pnp transistor in the CBIC-U2 technology, the channel layout is basically linear, i.e., one transistor after the other. Figure 11 shows a microphotograph of the 64-channel 6.8 mm x 3.1 mm chip. The IC contains 3600 transistors, 40 MΩ of resistance, and 450 pF of capacitance, which is a very large scale of integration for complementary bipolar technology. There are two staggered columns of input and output pads at each side of the IC. Bias and control signals are bussed across the IC, with pads on opposite sides, to allow direct chip-to-chip interconnect, as explained above. Global bias networks and bypass capacitors are located between bias pads. Four separate calibration/test lines are provided each connecting to the calibration capacitor of every fourth channel.

IV. MEASUREMENTS

A. Integrator

The integrator is a critical element in the analog signal processing since it predominantly defines the noise of the front-end electronics. A special test structure containing 16

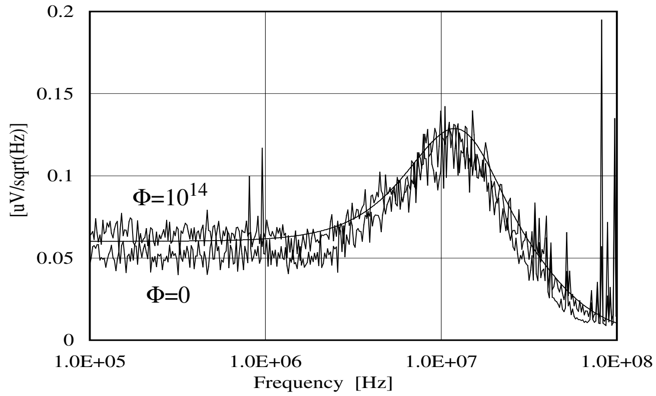


Figure 14. Integrator output noise voltage spectrum.

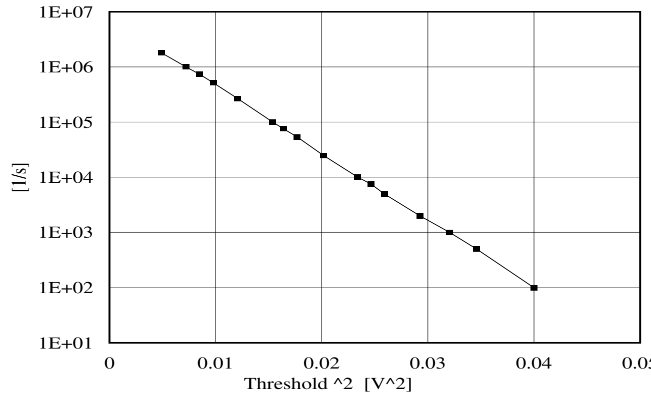


Figure 15. Measured rate of noise hits vs. threshold voltage.

integrators was laid out to permit complete characterization of this critical block.

The integrator has an open loop gain of 3600 (71 dB) and a gain-bandwidth product of 1 GHz (Figure 12). With a 15 pF source capacitance, the closed loop voltage gain has a peak value of 34 dB at 11 MHz. The open loop gain at the peaking frequency of the overall shaper is 40 dB. Comparing with Figure 8(a), the measured and simulated closed loop gain responses are in close agreement. Figure 13 shows the time response of the integrator (lower trace) to a 5 fC input signal (upper trace). The gain is approximately 2.2 mV/fC at a peaking time of 20 ns.

Of special interest is the noise performance of the integrator and its degradation with irradiation. To this end, a number of 16-integrator test structures were irradiated under bias at TRIUMF with 500 MeV protons to a fluence up to $\Phi=1\times10^{14}$ p/cm^2 representing an ionizing dose of approximately 4.5 Mrad. Figure 14 shows the output noise voltage spectrum in $\mu V/\sqrt{Hz}$ of a typical integrator before and after exposure with a 15 pF source capacitor. The smooth curve is the simulated performance. The first observation is the close agreement between measured and simulated results, which testifies on the completeness and robustness of SPICE models for the bipolar transistor. At high frequencies there is no significant change in the noise performance with irradiation, as expected. At low frequencies, the noise spectral density increases approximately by ~30%, indicating a drop in dc β of Q_1 consistent with previous measurements on single transistors. There was also no significant change in gain with irradiation. These measurements support the use of complementary bipolar technology up to the radiation hardness specification of $\Phi=1\times10^{14}$ cm^{-2} and beyond.

B. Analog front-end channel

To fully characterize the complete analog front-end channel a printed circuit board, including output buffers to boost the signal level, was fabricated. Wideband amplifiers with a total transimpedance gain of 14kΩ were used to bring the 35 μA output pulse to a 500 mV level. All measurements were performed at the nominal power dissipation of 1 mW/channel from a 3.5 V supply and with a 14 pF external source

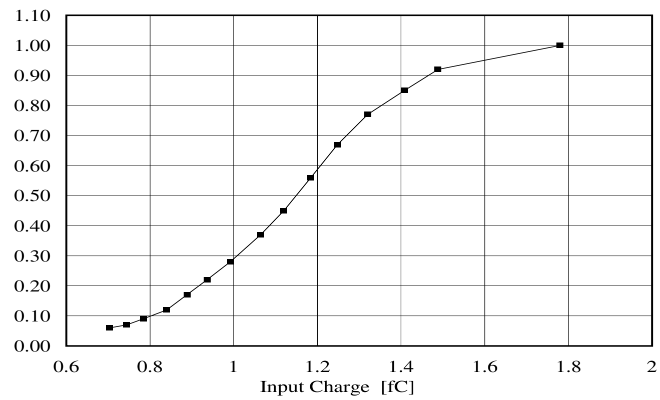


Figure 16. Measured counting ratio vs. input charge.

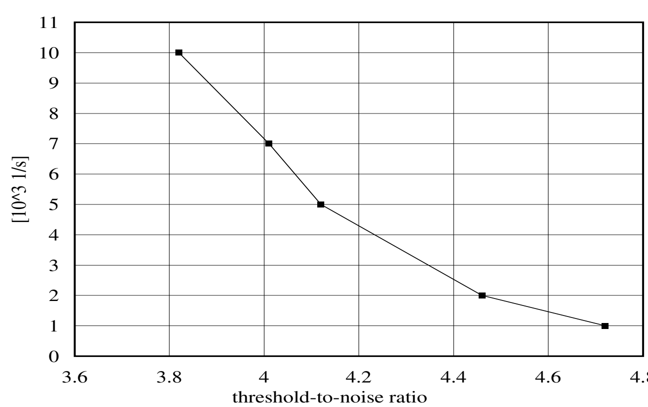


Figure 17. Measured rate of noise hits vs. threshold-to-noise

capacitor, unless otherwise noted. A bench-top commercial counter was used to perform the counting measurements. Although the front-end IC does not include an analog output, the variable threshold (combined with a measurement of the output pulse rate) forms a rudimentary pulse-height analyzer.

In the SDC silicon tracker [1] the average hit rate from particles in a strip is in the range of 1×10^4 to 2×10^5 s^{-1}. The threshold is set such that the rate of noise hits is lower than the rate of true hits. For a simple system consisting of an RC-CR filter followed by a threshold discriminator, the frequency of

$$f_n = e^{-V_t^2/2v_n^2} \cdot \frac{1}{4\sqrt{3} \cdot \tau} \qquad (1)$$

Transfer Gain	180	mV/fC
Equivalent Input Noise Charge		
C_d= 14 pF; single channel	1300	el. rms
C_d= 14 pF; multiple channel	1500	el. rms
Time Resolution ($1.25 \le Q_s \le 10$ fC); Q_t=1 fC		
with walk compensation	16	ns
without walk compensation	25	ns
Double Pulse Resolution (Q_s= 4 fC)	122	ns
Power Consumption (V_{cc}= 3.5 V)	1	mW

Table 2: Performance of the analog front-end IC.

noise hits, f_n, is given by equation (1) [4], where v_n is the rms system noise, V_t is the threshold and τ is the filter's shaping time. The shaper in the analog channel is not a simple RC-CR, so strict quantitative agreement with the above equation should not be expected, but the measured rate of noise hits for the analog front-end exhibits the exponential dependence with V_t^2, as shown in Figure 15.

To perform noise measurements, the threshold was set for a rate of noise hits f_n=2x10^3 s^{-1}. A signal rate of 500 ks^{-1} was used to allow counting down to a few percent. Figure 16 shows the ratio of output hits divided by the signal rate as a function of input charge. The rms equivalent noise charge was obtained by doing a regression and calculating the deviation from 84% (or 16%) to 50%. The equivalent charge threshold is given by the 50% point. With a 14 pF source capacitor the single channel noise is 1300 el. rms. The multiple channel noise is 1500 el. rms, as measured with 7 pF capacitors between adjacent channels. There is approximately a ±10% uncertainty in the accuracy of the results, dominated by capacitor tolerance. Figure 17 shows the measured rate of noise hits vs. threshold-to-noise ratio. The measurement indicates that a threshold-to-noise ratio of 4 results in a rate of noise hits of approximately 7x10^3 s^{-1}.

Figure 18 shows the amplified output waveform for input signals from 1.25 to 10 fC, with the threshold set at 1 fC. Figure 19 shows a detail of the same output waveform without (a) and with (b) walk compensation. With the walk compensation turned off, there is a monotonic delay response to signal amplitude with a 25 ns time resolution for the dynamic range of interest. With the walk compensation active the delay response, although non-monotonic, results in a 16 ns time resolution. As fabricated the compensation delay is less than intended, so that the potential improvement offered by this scheme is not fully exploited. Figure 18 also shows that the comparator gain is marginal, since pulses for $Q_s \le 1.5$ fC should saturate to make the timing response less sensitive to the subsequent digital threshold.

Table 2 summarizes the results of the analog front-end integrated circuit. A number of 64-channel ICs were also irradiated under bias at TRIUMF with 500 MeV protons. All 64 channels on the chip were functional after exposure to a fluence Φ=1x10^{14} p/cm^2. More detailed analysis of the post-radiation performance is underway.

V. SUMMARY AND CONCLUSIONS

A low-noise, low-power, high-bandwidth, radiation hard, silicon bipolar-transistor full-custom integrated circuit (IC) containing 64 channels of analog signal processing was developed for the SDC silicon tracker. The design objectives based on system requirements were briefly reviewed, a detailed description of the integrated circuit was presented and a comprehensive set of measurements was reported. Performance has been demonstrated after exposure to a fluence of 1x10^{14} cm^{-2} (500 MeV protons). This is the first production-oriented readout IC to demonstrate the analog front-end performance required by future high luminosity colliders, such as SSC and LHC. Higher density complementary bipolar processes now available allow a substantial reduction in die size to < 5 mm. These processes feature faster transistors, which offer the additional benefit of increased radiation resistance.

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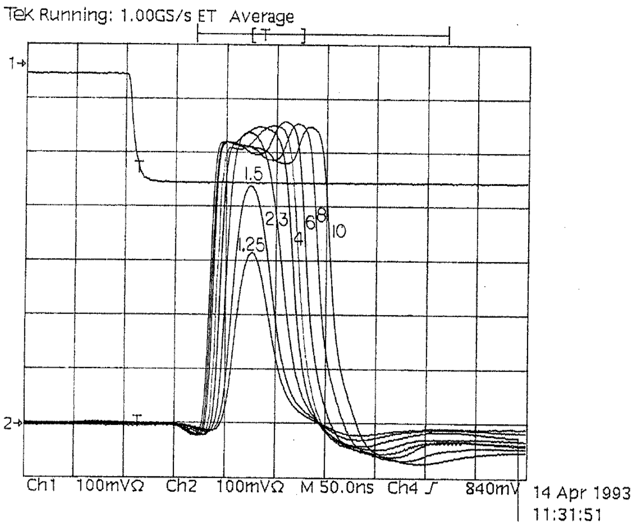
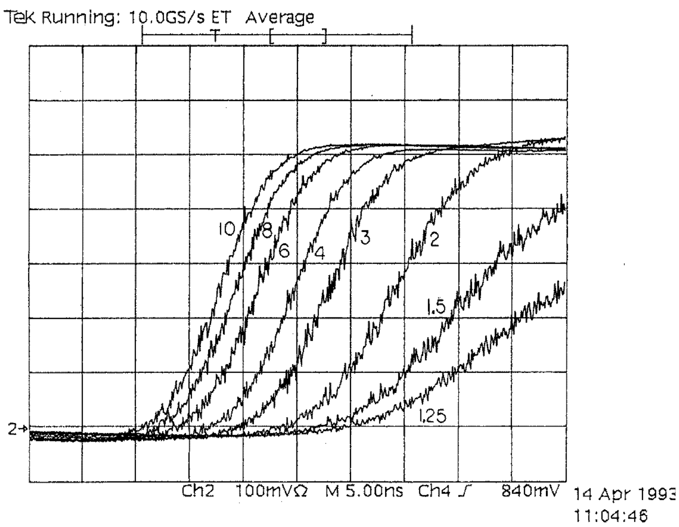
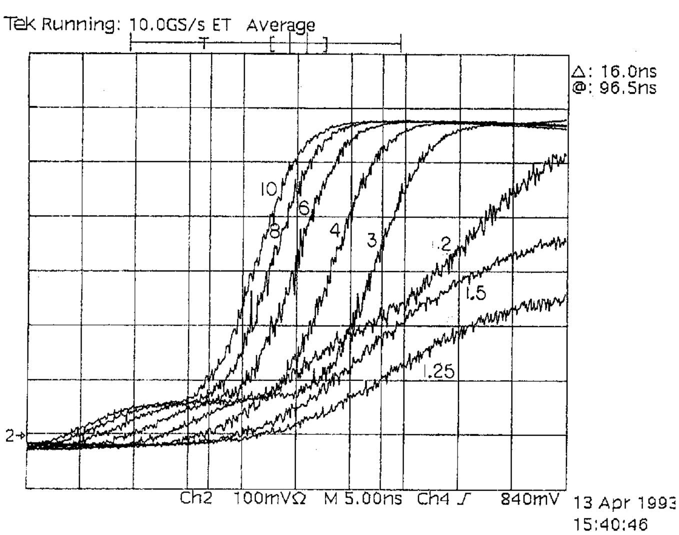


Figure 18. Amplified output waveform. $1.25 \leq Q_s \leq 10$ fC.



(a)



(b)

Figure 19. Detail of amplified output waveform. (a) without and (b) with walk compensation. $1.25 \leq Q_s \leq 10$ fC.