ABCD3T(A) chip wafer screening yield figures

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Contents

1 Scope

This document describes yield figures obtained during wafer screening of ABCD3T(A) chip [1] wafer lots delivered by ATMEL starting from July 2000. The goal of this document is to present yield figures for all wafers screened so far and their spread according to various technology variants performed by the foundry.
The wafer screening process is done in three different sites: CERN, SCIPP Univ. California Santa Cruz, RAL Rutherford Laboratories. Most of data presented comes from old CERN screening setup as at the time of screening other sites where preparing to do such task.
ABCD3T(A) wafers where delivered from ATMEL in 5 shipments of :

- box Z34685 (8 wafers) - July 2000
- box Z34685A (8 wafers + (2 wafers replaced later by ATMEL)) - November 2000
- box Z36459A (5 wafers), Z36459B (6 wafers), Z36459D (2 wafers), Z37277 (8 wafers), Z37277A (3 wafers) – February 2001
- box Z36459D (2 wafers), Z37277R (1 wafer) – March 2001
- box Z38850 (18 wafers + (2 send back to ATMEL)) – April 2001

It makes total of 59 wafers. Out of that number 32 wafers where screened and data was processed till now.

2 Definitions

In order to understand yield figures here are the definitions of terms used in this document:

- "Final yield" marked as y_f, is the ratio of number good (perfect) chips found on the wafer to total number of chips on the wafer.
- "Digital yield" marked as y_d, is the ratio of number chips with good digital part found on the wafer to total number of chips on the wafer.
- "Analogue yield" marked as y_a, is the ratio of number chips with good analog & digital parts found on the wafer to number chips with good digital part.
- "One unusable channel chip yield" marked as y_{ch1d}, is the ratio of number of chips with good digital part and all analog part good except one single channel to total number of chips on the wafer.
- "Two unusable channel chip yield" marked as y_{ch2d}, is the ratio of number of chips with good digital part and all analog part good except two channels to total number of chips on the wafer.

3 Screening procedure

During wafer screening at all screening sites the following procedure was applied (simplified description):

1. Wafer to be screened was inspected visually for presence of scratches on it surface with unaided eye.
2. It was then placed on the wafer-prober chuck and aligned with wafer-prober XY coordinates and probe-card In same time it was inspected with microscope for any misalignment of masks (basically metal-1 and metal-2), smoothness of contact pad surface in randomly selected wafer areas.
3. The wafer-screening equipment was verified then.
4. Over small (4-5) quantity of good chips from middle wafer area data was taken manually to find the most convenient StrobeDelay [1] parameter to run with.
5. Full wafer screening was started then.
6. After successful end wafer was taken away from wafer-prober and raw data was sent to processing computer.
7. Then the offline analysis was done according to description in "Test specification document" [2]

With old CERN setup it took from 28-38h to screen one wafer. With new setup [3] (i.e. LBNL hardware) it takes 11h.

4 Yield figures

The yield figures for all screened wafers are presented in Table 1.

Wafer name	*wid*	y_f	Y_{ch1d}	Y_{ch2d}	y_a	y_d	Remarks
CERNOLD-Z34685	2	**9.4%**	11.3%	6.6%	27.3%	**34.4%**	in spec.
CERNOLD-Z34685	3	**3.5%**	3.9%	4.3%	12.7%	**27.7%**	in spec.
CERNOLD-Z34685	4	**4.7%**	6.6%	7.4%	12.1%	**38.7%**	in spec.
CERNOLD-Z34685	5	**26.2%**	25.0%	11.7%	37.6%	**69.5%**	in spec.
CERNOLD-Z34685	6	**3.1%**	6.3%	3.1%	11.4%	**27.3%**	in spec.
CERNOLD-Z34685	8	**3.5%**	6.6%	1.6%	13.3%	**26.6%**	in spec.
CERNOLD-Z34685	9	**12.9%**	10.6%	2.7%	47.1%	**27.3%**	in spec.
CERNOLD-Z34685	10	**12.1%**	14.8%	4.7%	30.7%	**39.5%**	in spec.
CERNOLD-Z34685A	11	**11.3%**	12.1%	11.7%	22.1%	**51.2%**	"corner run"
CERNOLD-Z34685A	12	**7.8%**	11.7%	8.6%	18.2%	**43.0%**	"corner run"
CERNOLD-Z34685A	14	**9.4%**	11.7%	6.6%	27.0%	**34.8%**	"corner run"
CERNOLD-Z34685A	15	**5.5%**	3.1%	3.9%	26.4%	**20.7%**	"corner run"
CERNOLD-Z34685A	16	**7.8%**	3.5%	0.8%	42.5%	**18.4%**	"corner run"
CERNOLD-Z34685A	17	**10.2%**	9.4%	3.1%	31.3%	**32.4%**	"corner run"
CERNOLD-Z34685A	19	**7.8%**	7.0%	3.9%	31.2%	**25.0%**	"corner run"
CERNOLD-Z34685A	20	**8.6%**	4.7%	1.2%	44.9%	**19.1%**	"corner run"
CERNOLD-Z36459A	3	**25.4%**	11.3%	5.5%	44.2%	**57.4%**	in spec.

CERNOLD-Z36459A	4	**17.2%**	14.1%	9.8%	31.4%	**54.7%**	in spec. (valley of death found)
CERNOLD-Z36459A	5	**31.3%**	16.4%	7.4%	48.2%	**64.8%**	in spec.
CERNOLD-Z36459A	6	**30.5%**	21.9%	5.5%	45.1%	**67.6%**	in spec.
CERNOLD-Z36459B	12	**14.1%**	12.5%	10.2%	23.4%	**60.2%**	thin tox over nmos
CERNOLD-Z36459B	18	**22.3%**	11.3%	5.1%	47.9%	**46.5%**	thin tox over nmos
CERNOLD-Z37277	7	**8.2%**	9.8%	7.0%	19.4%	**42.2%**	high res. material problem
CERNOLD-Z37277	15	**6.6%**	5.9%	7.0%	14.4%	**46.1%**	high res. material problem
CERNOLD-Z37277A	6	**8.6%**	9.4%	5.5%	26.5%	**32.4%**	high res. material problem
CERN-Z38850	3	**6.3%**	7.4%	4.7%	18.2%	**34.4%**	
CERN-Z38850	4	**6.6%**	15.2%	9.4%	15.5%	**43.0%**	
SCIPP-Z38850	5	**13.3%**	16.4%	5.9%	29.6%	**44.9%**	
SCIPP-Z38850	8	**16.4%**	23.4%	9.8%	25.9%	**63.3%**	enhanced emitter contact
CERN-Z38850	13	**20.7%**	13.7%	5.9%	40.8%	**50.8%**	new EPI
CERN-Z38850	15	**27.3%**	18.0%	6.3%	51.8%	**52.7%**	new EPI
SCIPP-Z38850	18	**38.3%**	19.1%	5.5%	55.7%	**68.8%**	new EPI/enhanced emitter contact

Table 1 Yield figures of 32 wafers screened, where "*wid*" is wafer number id and y_f, y_{ch1d} , y_{ch2d} , y_a , y_d as defined in section 2.

Wafers tested with old CERN setup are prefixed CERNOLD, wafers tested at CERN with new hardware from LBNL are prefixed CERN, wafers tested at Univ. Santa Cruz are prefixed SCIPP. In the "Remarks" field one can find special note concerning given wafer. Wafers marked Z34685 were from July 2000 delivery, Z3468A was the "corner run" delivered November 2000, lots Z37277, Z37277A, Z36459A and Z36459B were delivered January-February 2001. The new epi/old epi vendor split and emitter contact enhancement split lot Z38850 was delivered in April 2001.

5 Wafer split description

The yield obtained on all wafer has to be analysed in terms of foundry delivered electrical parameters and wafer specifications. This immediately divides set of wafers into 4 groups:

- wafers that ATMEL has claimed in spec, i.e. all electrical parameters are inside specification for this technology and based on normal EPI layer subcontractor (lots Z34685 , Z36459A, Z38850 wafers 1-11)

- “corner run” . Wafers from this lot were grouped in pairs (i.e. 5 groups) and processed with different technological parameters to find if there is certain set of these parameters that gives better final yield and if there is any other yield dependence on wafer splits (lot Z34685A). Wafers were fabricated with normal EPI layer subcontractor.
- out of technology specification wafers delivered by ATMEL based on normal EPI subcontractor (lots Z36459B, Z37277, Z37277A)
- wafers based on new EPI layer subcontractor (lot Z38850 wafers 12-19)

The last delivery from ATMEL (lot Z38850) besides split of new/old EPI vendor was also split by:

- normal emitter opening oxide thickness
- thin emitter opening oxide thickness

Which makes 4 groups of wafers in that lot. All splits are summarized in table 2.

Wafer name	*wid*	*in spec*	*corner run*	*new/old EPI layer*	*thin/normal emitter opening oxide*
CERNOLD-Z34685	2	yes	no	old	normal
CERNOLD-Z34685	3	yes	no	old	normal
CERNOLD-Z34685	4	yes	no	old	normal
CERNOLD-Z34685	5	yes	no	old	normal
CERNOLD-Z34685	6	yes	no	old	normal
CERNOLD-Z34685	8	yes	no	old	normal
CERNOLD-Z34685	9	yes	no	old	normal
CERNOLD-Z34685	10	yes	no	old	normal
CERNOLD-Z34685A	11	no	yes	old	normal
CERNOLD-Z34685A	12	no	yes	old	normal
CERNOLD-Z34685A	14	no	yes	old	normal
CERNOLD-Z34685A	15	no	yes	old	normal
CERNOLD-Z34685A	16	no	yes	old	normal
CERNOLD-Z34685A	17	no	yes	old	normal
CERNOLD-Z34685A	19	no	yes	old	normal
CERNOLD-Z34685A	20	no	yes	old	normal
CERNOLD-Z36459A	3	yes	no	old	normal
CERNOLD-Z36459A	4	yes	no	old	normal
CERNOLD-Z36459A	5	yes	no	old	normal
CERNOLD-Z36459A	6	yes	no	old	normal
CERNOLD-Z36459B	12	no	no	old	normal
CERNOLD-Z36459B	18	no	no	old	normal
CERNOLD-Z37277	7	no	no	old	normal
CERNOLD-Z37277	15	no	no	old	normal
CERNOLD-Z37277A	6	no	no	old	normal
CERN-Z38850	3	not known	no	old	normal
CERN-Z38850	4	not known	no	old	normal

SCIPP-Z38850	5	not known	no	old	normal
CERN-Z38850	8	not known	no	old	thin
CERN-Z38850	13	not known	no	new	normal
CERN-Z38850	15	not known	no	new	normal
SCIPP-Z38850	18	not known	no	new	thin

Table 2 Summary of various splits of wafers already screened.

The “corner run” (lot Z34685A) splits were based on fine tuning of several ATMEL technology parameters:

- high/nominal/low transistor threshold voltage (VTx)
- oversize/nominal/undersize POLY layer
- nominal/over doped implant base

Summary of “corner run” splits are presented in table 3.

Wafer ID (Z34685A)	VTs	POLY layer	Rext (imp. base)
11,12	high (+)	nominal	nominal.
13,14	low (-)	nominal	nominal
15,16	nominal	undersized (-)	(-) over doped
17,18	nominal	oversized (+)	(-) over doped
19,20	low (-)	undersized (-)	nominal

Table 3 Summary of “corner run” wafer groups.

On wafers 13 and 18 of this lot, dead regions were found after screening. Which in case of wafer 13 was impurities confirmed by later visual inspection. In case of wafer 18 the misalignment of masks M1,M2 & VIA of more than 3um on wafer edges where found. These two wafers were sent back to foundry and have been replaced by wafers 14 and 16. Wafer 17 had two 4-6 cm long scratches along it’s surface, but was held at CERN as reference (golden) wafer.

6 Summary

By careful reading of wafer yield table (table 1) one can conclude:

- From yield figures for “corner run” one can not deduct any yield dependence over technology parameter fine tuning., which prove chip design to be robust against process variations.
- The overall wafer yield is far lower from expected “minimum yield” even if we include wafers that were claimed by ATMEL as “in spec” only.
- The new foundry option, i.e. new EPI layer subcontractor and enhanced emitter contact looks promising, but one should be very careful in interpretation as only one wafer of this split was tested and analysed till now.

References

[1] "ABCD3T Chip, Project Specification, Version V1.2"
[2] W. Bialas, W. Dabrowski, V. Fadeyev,C. Lacasta, J. Kaplon "Testing specification for the wafer screening. Project Name: ABCD3T ASIC Version: V2.1, 25 June, 2001"
[3] A. Ciocio and V. Fadeyev "Test System for ABCD3T Wafer Screening" June 20, 2001