

Testing specification for the wafer screening
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1 Scope

This document describes the environment and requirements for testing of the ABCD3T chip for readout of silicon strip detectors for ATLAS SCT. It is meant to provide pass/fail criteria for each chip based on analysis of data taken during the wafer screening of the ABCD3T chips.

The wafer testing system should complete two tasks:

- Qualification of good chips to be delivered for the SCT detector (Database filled with all electrical parameters and coordinates of the chip on the wafer to check that chips are delivered according to the specification).
- Yield analysis, which is a part of the design validation and control of the process stability during the production (generation of bin files, which are used as inputs for the bin analysis performed in the foundry (ATMEL)).

The architecture of the ABCD3T chip and full specification is described in the “ABCD3T Chip, Project specification, Version V1.2” document [1]. The simplified block diagram of the ABCD3T chip is shown in figure 1.

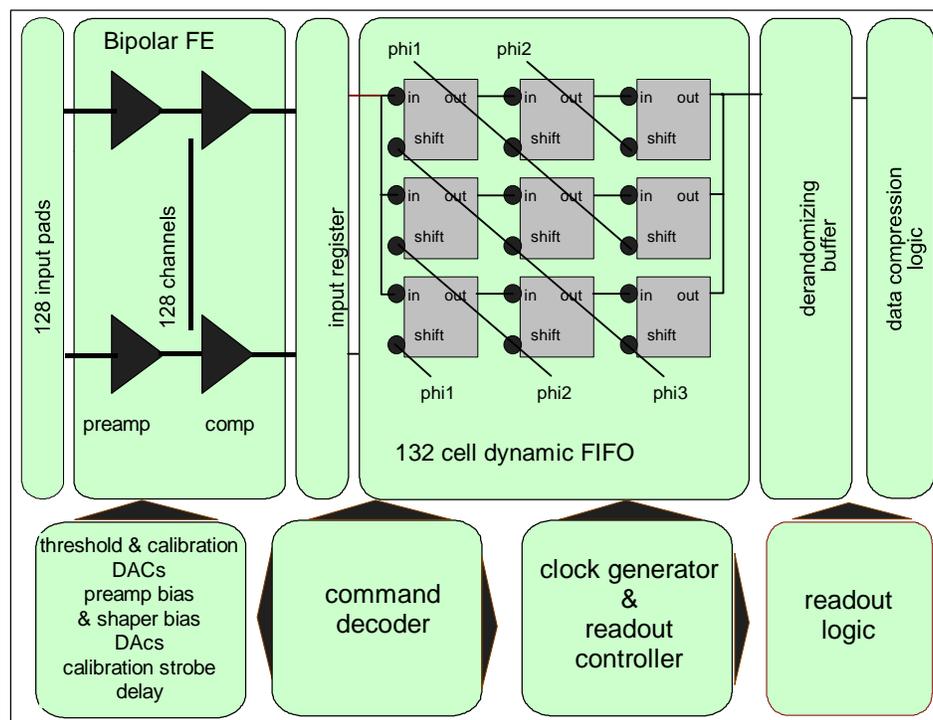


Figure 1: Block diagram of the ABCD3T chip.

Functionally the ABCD3T chip can be split in to two main blocks:

- Analogue front-end containing 128 channels of fast transimpedance amplifiers and comparators, digital-to-analogue converters and calibration circuit (about 30000 BiCMOS devices placed on 5mm^2)
- Digital part containing the input register, pipeline, derandomizing buffer, command decoder, readout logic, and threshold & calibration control (about 200000 CMOS devices laid out on 46mm^2 silicon area).

The functionality of the analogue part of the chip is tested using internal calibration circuitry. Each channel has an internal calibration capacitor connected to its input for purposes of simulating a "hit" strip. The calibration capacitors are charged by an internal chopper circuit, which is triggered by a command. Every fourth channel can be tested simultaneously with group selection determined by two binary coded calibration address inputs (CALD0, CALD1). The strobe and the address signals are delivered from the control block. The voltage applied to the calibration capacitors by the chopper is determined by an internal DAC. A tuneable delay of the calibration strobe with respect to the clock phase covering at least two clock periods is provided.

The whole digital part of the chip is tested separately using test vectors which stimulate the inputs of the digital circuitry and contrast the output against the simulated chip response.

Internal testability features implemented in the design allow testing of the analogue performance via digital control signals adhering to the LVDS standards. This solution offers the possibility of precise measurement of analogue parameters during the wafer screening.

The calibration signals processed in the amplifier and comparator can be read-out only through the digital part of the chip. A consequence of this is that an estimation of the yield of the analogue part can only be performed for that subset of chips which pass the digital tests.

2 Reference documents

1. ABCD3T Chip, Project Specification, Version V1.2
2. Description of the LBNL Tester hardware: <http://www-atlas.lbl.gov/strips/>
3. Description of the Wafer Screening Data Analysis Software: <http://ific.uv.es/~lacasta/WaferScreening/>
4. W. Dabrowski, et al., "Fast Bipolar Front-end for Binary Readout of Silicon Strip Detectors", Nuclear Instruments and Methods A 350 (1994), 548.
5. Description of the ROOT package: <http://root.cern.ch>
6. W. Dabrowski, J. Kaplon, R. Szczygiel "SCT128B a prototype chip for binary readout of silicon strip detectors", Nuclear Instruments and Methods in Physics Research A 421 (1999) 303-315
7. W. Dabrowski, et al., "Performance of the Binary Readout of Silicon Strip Detectors Using the Radiation Hard SCT128B Chip", IEEE, Trans. Nucl. Sci. Vol. 45, No.3 (1998), 310.
8. W. Dabrowski, et al., "The ABCD Binary Readout Chip for Silicon Strip Detectors in the Atlas Silicon Tracker", Proc. of the Fourth Workshop on Electronics for LHC Experiments, Rome, September 21-25, 1998, CERN/LHCC/98-36, p. 175.
9. ABCD2T/ABCD2NT ASIC, Project Specification V 2.1.

3 Wafer Screening System

The test apparatus for wafer screening is based on a probe station with a fully motorised chuck stage whose movement is controlled through a GPIB interface. The data acquisition is provided by the LBNL-developed dedicated test system, composed of a VME board, probe card and two PCB boards in-between containing chips for timing delays and signal level variation. The VME board has an FPGA controlling the data flow in the system. The FPGA contains logical algorithms for histogramming the threshold scan data in hardware and operating the test vectors in burst mode, when only the results of comparison of the chip data and the simulation are read out [2]. The vacuum (which fixes the wafers to the chuck) is being checked by a probe station specific setup during wafer probing. The whole system is controlled by a dedicated program written in C++ and running on a PC under Windows NT. The program controls the VME and the GPIB buses. It builds the commands to carry out the tests, reads out the VME modules, controls all the movements of the wafer prober, configures the power supplies, reads the power consumption and DC voltages from all test pads of the digital-to-analogue converters. Probe movements are carefully controlled and the entire system stops if any disagreement is found between the programmed and monitored coordinates or if the vacuum fails.

3.1 Reliability issues

The high number of test vectors, long duration of the probing (1-2min) and complexity of the tests require a very reliable connection between the chip and the probe needles. Since we are using a custom design probe card with it is not possible to check the connections between the needles and the probed pads as in standard industrial probers by taking the DC characteristic of the protection devices before the execution of real tests. The biggest problem for the reliability of the connection is the oxidation and mechanical degradation of the needles during the probing. Depending on the material used for the needles (specification obtained from the probe card vendor) cleaning of the probe card needles is required every 30 (50) wafers. Since there is no way to check the quality of the connections between the chip and the probe card on-line it is necessary to check this during off-line data analysis. The proposed method is to look at the result of a scan of digital test block for different power supply voltages and frequencies. The specified scan is performed to extract the basic output parameters for digital tests:

- minimum Vdd at 40MHz BCO clock for 100% efficiency in the digital tests
- maximum frequency for 100% efficiency in the digital tests Vdd=4V.

These two parameters characterising the speed margin of the chips depend on two factors:

- actual parameters of the CMOS devices coming from the given run (slow, typical or fast corner of the process)
- quality of the connection between the needles and probe pads (higher resistance for the connection implies higher voltage drop on the power supply pads)

Analysing the number of chips passing the digital tests executed for different bias conditions (value of Vdd and BCO frequency) it is possible to plot the yield versus Vdd figure for a given wafer screened during one test run. An example of such a plot is shown in Figure 2. In the yield figure one can distinguish two regions:

- The flat part of the figure where the number of chips passed the tests is constant above some value of the Vdd. The fluctuations in this region indicate problems possibly due to unreliable chip contact.
- The transition region, where the number of chips passing the tests is changing. Widening of the transition region and moving it to the higher Vdd value indicates a problems with the probe contacts (assuming that wafers from the same run have the same speed performance).

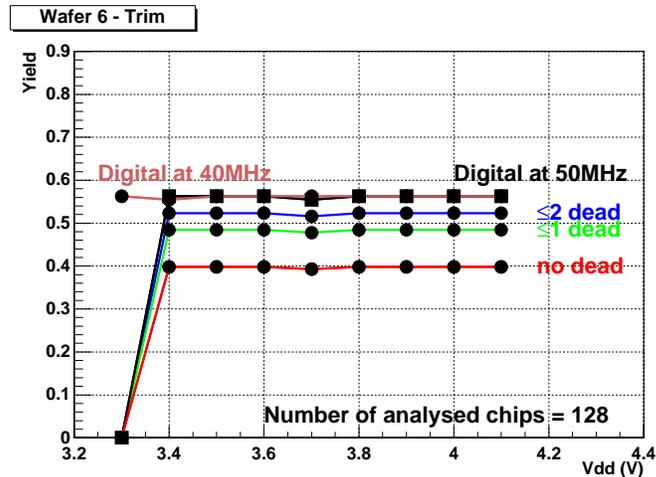


Figure 2: Digital and analogue yield versus Vdd for 40 and 50MHz BCO clock.

3.2 Quality of the analogue measurements

The measurement method to obtain the analogue parameters (gain, noise and offset) for the chip is fully described in reference [6]. The gain, offset and noise of the front-end can be evaluated by scanning the discriminator threshold for a given input charge applied from the internal calibration circuitry. For each threshold value a series of pulses is applied and the fraction of pulses which fire the comparator is measured. The threshold scan for a given input signal gives the so-called S-curve, i.e. counting rate as a function of the threshold. Provided the noise has a Gaussian amplitude distribution, the S-curve is described by the complementary error function. The 50% points of the S-curve correspond to a threshold equal to the signal amplitude while the width of the S-curve contains information about the r.m.s. value of noise. By performing these measurements for several values of the input charge one can extract the gain of all the circuitry preceding the discriminator and the discriminator input offset.

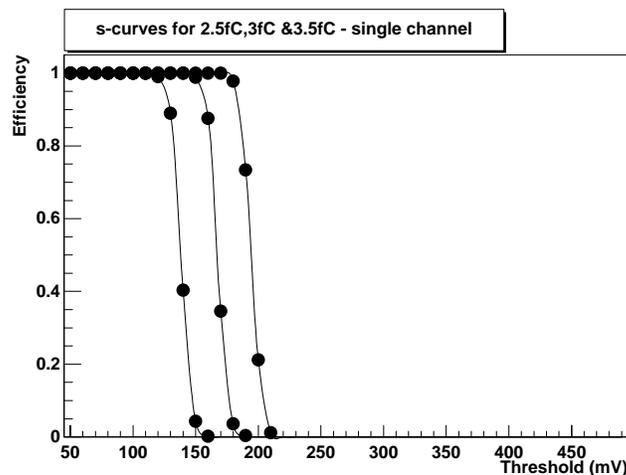


Figure 3: Example of the S-curves taken with 500 triggers (normalized to 1)

This measurement of the analogue performance requires the acquisition of clean S-curves (fitting well to the complementary error function) which means there should be a low level of excess noise and interference from the digital signals. Satisfying that requirement is essential to provide reliable fits during data analysis. Any crashing fit of a single S-curve to the complementary error function during offline data analysis will result in the generation of an artificial defect in the analogue part of the chip. For this reason, it is highly desirable to check the quality of fits in the case where chips show single defects in the analogue part only. Assuming a trigger rate in the range of 100-500 per scanned point it is necessary to keep the saturated noise occupancy (independent of the threshold) below 10^{-3} . Example of S-curves for one of the channels of the tested chips is shown in Figure 3. The quality of data taken during wafer screening should provide a full characterization of the tested ABCD3T chips including also the noise measurement performed with some accuracy. The excess noise caused by the non-

optimum assembling of the chip during probing should not be higher than the electronic noise coming from the input device (base current of the input transistor plus feedback resistor plus noise related to the parasitic input capacitance of the bonding pad). This gives a limit of about $1200e^-$ ENC of noise for a nominal bias current in the input BJT ($220\mu A$). The typical figure of gain and output noise obtained with an active probe card (CERN apparatus) is shown in figures 4 and 5 respectively. The calculated ENC is in the range of $1000e^-$, which has to be compared with $700e^-$ noise obtained for the chip mounted on a hybrid and under the same bias conditions. The RMS spread of the noise between channels is only $50e^-$. This result allows us to make a reliable cut when looking for noisy channels in the analogue FE part (the value used for the cut is $2000e^-$).

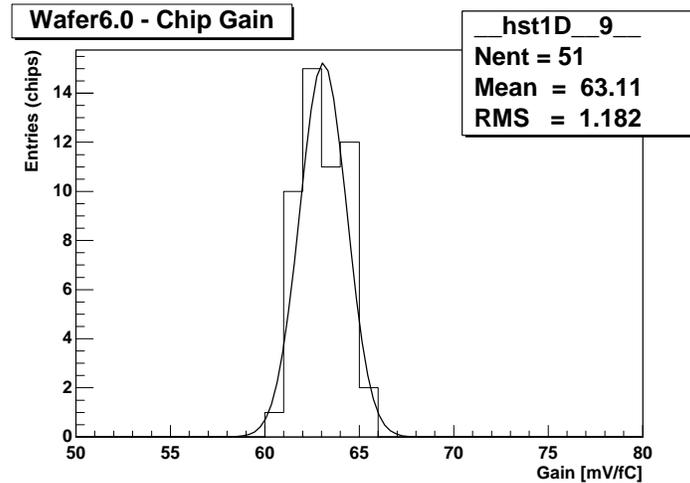


Figure 4: Distribution of the mean values of the gain for one wafer from batch Z31122 (for the accepted chips)

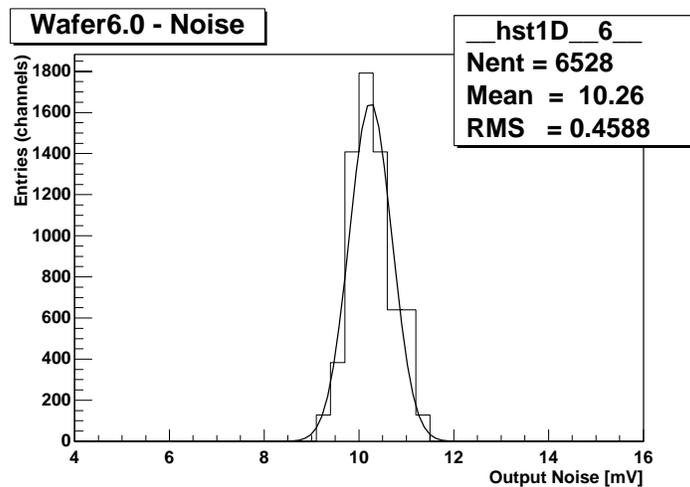


Figure 5: Distribution of the output noise for one wafer from batch Z31122 (for the accepted chips)

4 Flow of tests

The wafer prober system provides a full parameterization of the ABCD3T chips. The test flow is shown in figure 6. The test starts with the configuration register test. All the chips passing this basic digital test for the nominal condition of power supply and speed are examined and the results are saved for off-line analysis and tagging. Skipping the chips failing the CONFIG REGISTER test accelerates the screening process. All remaining chips are tested without stopping due to the failure of any one test. This approach is driven by the necessity of having full information about the wafer in order to control the final yield and distribution of defects in various blocks of the chip.

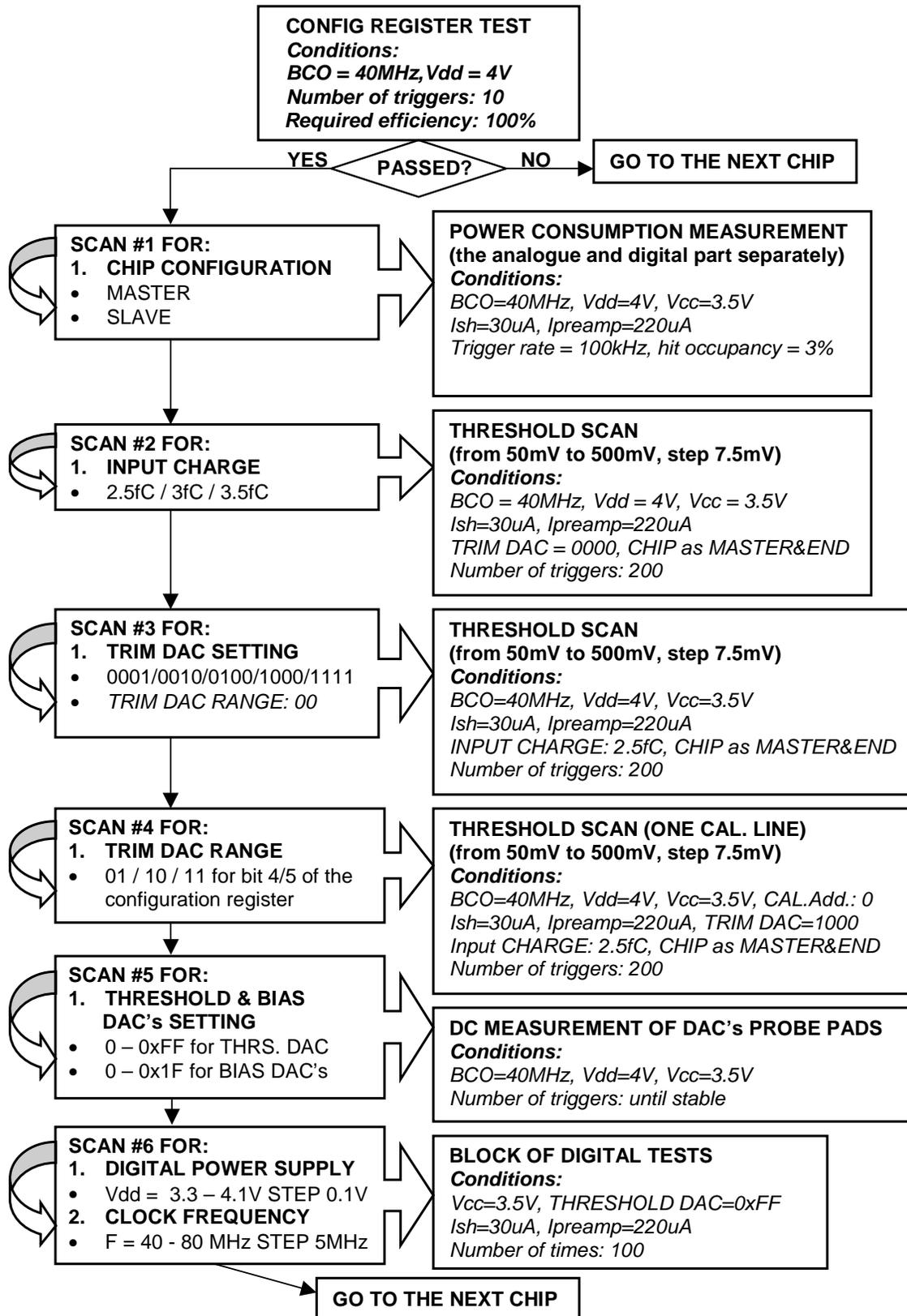


Figure 6: Flow of tests executed during probing of a single ABCD3T chip.

The power consumption of the chip is measured separately in analogue and digital parts of the chip for nominal speed, bias, trigger rate and hit occupancy conditions, both in MASTER and SLAVE mode of operation. Analogue parameters (gain, noise, offset, and characteristic of TRIM DAC) are obtained by scanning the threshold for several levels of calibration signals. The characteristics of all digital-to-analogue converters are measured using the test probe pads. A number of tests are made to check all digital functionality. The full set of those tests is performed for different values of Vdd and frequency in order to extract the speed margins of the devices

5 Power consumption measurement

The power consumption of both digital and analogue parts of the chip is measured. To simulate the nominal working conditions for the ATLAS SCT occupancy and L1 trigger rate, the measurement is done applying a 100kHz trigger with an occupancy of 3% (hits in 4 channels). ABCD3T chips with power consumption outside the standard distribution will be rejected due to possible weakness of some parts and potential limited reliability. The typical distribution of the power consumption of the ABCD chips working as slave or master for one wafer from batch Z31122 is shown in figure 7.

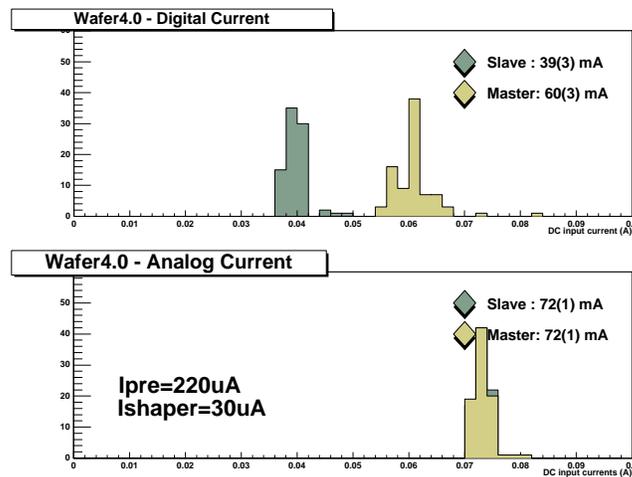


Figure 7: Distribution of the power consumption of the ABCD chips from batch Z31122.

SETTINGS	CHIP configuration	END EDGE_ON DATA_COMPRESSION_01X DATA_TAKING_MODE SELECT_0		
	CHIP bias	Ipreamp	220 μ A	
		Ishaper	30 μ A	
		Vcc	3.5 V	
		Vdd	4 V	
		BCO	40 MHz	
		Threshold DAC	0xFF	
	TRIM DAC	Value	0000	
Range		00		
CHIP address	Programmed = 1			
COMMAND	Issue Calibration Pulse + 131 BCO delay + L1 trigger			
SCANS	LOOPS	1. Chip configuration = {MASTER, SLAVE}		
	Trigger rate	100 kHz		

Table 1: Power consumption measurement (SCAN #1, Figure 6).

6 Description of the analogue tests

During wafer screening all functions related to signal processing should be exercised and measured. The gain, offset and noise for each channel should be measured and stored in data file. During the wafer screening the measurement of the time walk is too time consuming. In order to capture those chips with a timing problem all threshold scans should be done with edge detection circuitry ON and data compression mode 01X. For each wafer the timing applied via calibration delay register should be verified. This can be accomplished by a threshold scan in EDGE mode and comparison of the offset extracted from response curves with the leading edge of the S-curves (for good timing these two values should be very close to each other).

6.1 Gain, offset and noise characterization

The goal of the test is to determine the basic analogue parameters of the front-end: gain, noise and discriminator offset for each electronic channel. For this purpose threshold scans for four different input charges are done for each channel in the chip. The input transistor current and shaper current are set to nominal values and a 40MHz BCO clock drives the chip. Four S-curves per channel are fitted to a complementary error function. From the 50% points the gain curve is extracted and fitted to a straight line. The gain and the offset are taken as the slope and offset of the linear fit respectively. The electronic noise is obtained for each pulse from S-curve fit.

SETTINGS	CHIP configuration	MASTER END EDGE_ON DATA_COMPRESSION_01X DATA_TAKING_MODE SELECT_0		
	CHIP bias	lpreamp	220 μ A	
		lshaper	30 μ A	
		Vcc	3.5 V	
		Vdd	4 V	
		BCO	40 MHz	
	TRIM DAC	Value	0000	
		Range	00	
CHIP address	Programmed = 1			
COMMAND	Issue Calibration Pulse + 131 BCO delay + L1 trigger			
SCANS	LOOPS	<ol style="list-style-type: none"> 1. INPUT CHARGE = {2.5, 2.875, 3.625, 4.0} fC 2. CALIBRATION ADDRESS = {0,1,2,3} 3. THRESHOLD = [50mV – 500mV] step 7.5mV 		
	No. of triggers	200		

Table 2: Gain, noise and offset characterisation (SCAN #2, Figure 6).

6.2 Characterization of the TRIM DAC's

In order to compensate channel-to-channel variation of the discriminator offset each channel is provided with a trim DAC of 4-bit resolution. Each channel can be addressed individually and the threshold correction can be applied channel by channel. The range of the trim DAC can be selected with two bits in the configuration register. For the TRIM DAC characterisation, a scan for a selected combination of settings is done for each electronic channel and for a fixed calibration pulse (2.5fC). Applying the same analysis described as for the gain and offset measurement, an overall characteristic of the TRIM DAC is obtained. The measurement is done for the basic range of the TRIM DAC (00). The measurement point for the TRIM DAC value = 0000 is taken from the previous measurement of the gain and offset (to limit the number of points in the scan).

SETTINGS	CHIP configuration	MASTER END EDGE_ON DATA_COMPRESSION_01X DATA_TAKING_MODE SELECT_0		
	CHIP bias	Ipreamp	220 μ A	
		Ishaper	30 μ A	
		Vcc	3.5 V	
		Vdd	4 V	
		BCO	40 MHz	
	Input Charge	2.5 fC		
	TRIM DAC	Range	00	
CHIP address	Programmed = 1			
COMMAND	Issue Calibration Pulse + 131 BCO delay + L1 trigger			
SCANS	LOOPS	1. TRIM DAC VALUE = {0001, 0010, 0100, 1000, 1111} 2. CALIBRATION ADDRESS = {0,1,2,3} 3. THRESHOLD = [50mV – 500mV] step 7.5mV		
	No. of triggers	200		

Table 3: Characterisation of the TRIM DAC's (SCAN #3, Figure 6).

6.3 Characterization of the TRIM DAC range

The range of the trim DAC can be selected with two bits in the configuration register (see Table 3.10b in ref. [1]). This is to cover the offset spread, which is expected to increase after irradiation. There are four selectable ranges of the TRIM DAC.

Trim DAC range Bit 1	Trim DAC range Bit 0	Trim DAC range	Trim DAC step
0	0	0 mV – 60 mV	4 mV
0	1	0mV –120 mV	8 mV
1	0	0mV –180 mV	12 mV
1	1	0mV –240 mV	16 mV

Table 4: Trim DAC range selection.

Since the goal of this measurement is to check the range of the TRIM DAC which is a common factor for all channels only one calibration line is used (calibration address 0). The scan for the TRIM DAC RANGE setting is performed for one TRIM DAC value (1000) and one calibration charge (2.5fC). The measurement point for TRIM DAC RANGE = 00 is taken from the previous scan. The TRIM DAC RANGE is calculated as an average of the values obtained from 32 scanned channels (calibration address 0).

SETTINGS	CHIP configuration	MASTER END EDGE_ON DATA_COMPRESSION_01X DATA_TAKING_MODE SELECT_0		
	CHIP bias	Ipreamp	220 μ A	
		Ishaper	30 μ A	
		Vcc	3.5 V	
		Vdd	4 V	
		BCO	40 MHz	
	CALIBRATION address	0		
	Input Charge	2.5 fC		
	TRIM DAC	Value	1000	
CHIP address	Programmed = 1			
COMMAND	Issue Calibration Pulse + 131 BCO delay + L1 trigger			
SCANS	LOOPS	1. TRIM DAC RANGE = {01, 10, 11} 2. THRESHOLD = [50mV – 500mV] step 7.5mV		
	No. of triggers	200		

Table 5: Characterisation of TRIM DAC range (SCAN #4, Figure 6).

7 Measurement of the characteristics of the Digital-to-Analogue Converters

The ABCD3T chip has 3 main DACs, which must be tested:

- Threshold DAC (8 bits)
- Input transistor current DAC (Ipreamp - 5 bit)
- Shaper current DAC (Ishaper – 5 bit)

The chip incorporates one additional 8 bit DAC for the calibration pulse height, which is not directly tested and its failure will result in a deficient analogue performance. In order to check the characteristic of the DAC a full scan across the DAC settings is done and the DC levels provided by the chip at its test pads are readout. This allows a measurement of the linearity error, as shown in figure 8, where the relative deviation from linearity with respect to the DAC range is also depicted.

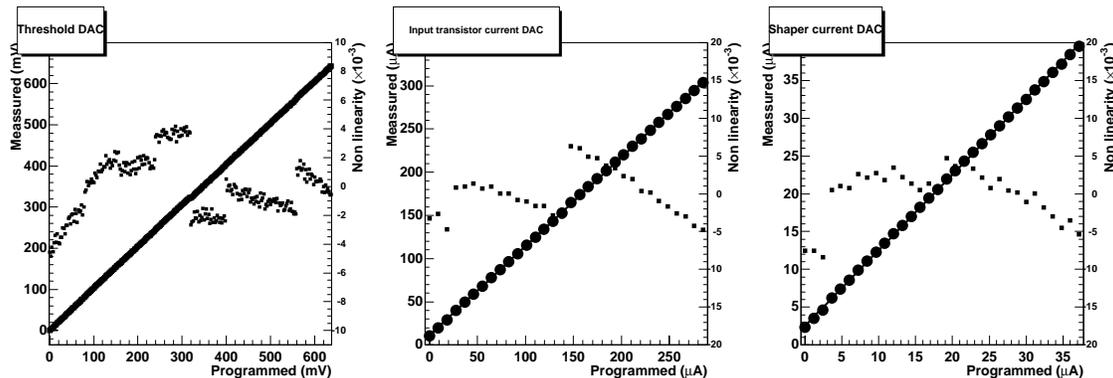


Figure 8: Linearity of the threshold and bias DACs. The round bullets show the DAC characteristic. The small square bullets show the deviation from linearity relative to the range of the DAC. Its scale is shown on the right axis.

The output of the threshold DAC is available directly at the pads VTHN and VTHP ($V_{\text{threshold}} = V_{\text{THP}} - V_{\text{THN}}$). The outputs of the preamplifier and shaper bias DACs could be tested on the pads IP_PROBE and

IS_PROBE respectively. The conversion between value of the current at the DAC output and value of the voltage at the probe pad are described by following formulas:

$$V_{IP_PROBE}[V] = I_{PREAMP}[A] \times 250 \times (R_{RLV_NORM}/R_{RBXB_NORM})$$

$$V_{IS_PROBE}[V] = I_{SHAPER}[A] \times 1000 \times (R_{RLV_NORM}/R_{RBXB_NORM})$$

Where RRLV_NORM and RRBXB_NORM are normalised values for RLV and RBXB type resistors (actual value divided by the nominal value) and they may fluctuate from lot to lot due to the process variations. For nominal values of the parameters (resistors, Vbe and temperature) the range of the preamplifier bias DAC is about 300uA which corresponds to the 75mV signal at the IP_PROBE pad. The range for the shaper bias DAC is about 38uA which is equivalent to 38mV signal at the IS_PROBE pad.

8 Description of the block of digital tests

A number of tests are applied to check all the digital functionality of the chip. The main characteristics to ascertain are related to chip control, inter-chip communication and data compression. All the tests make extensive use of two testing tools provided by the ABCD3T chip: pulsing the input register or generating output pattern through the mask register. To evaluate the performance of the chip in the different tests, four different patterns with a length of 128 bits are injected:

- a sequence of 128 ones (mask #1)
- a sequence of 010101...01 (mask #2)
- a sequence of 101010...10 (mask #3)
- a sequence of all zeros (mask #4)

For some tests, a fixed mask with random bits is used.

To determine the speed margins and the radiation resistance of the device, the described block of digital tests is performed for different values of frequency and power supply (SCAN #6, Figure 6). A chip passes a test if the output data match the simulated response, as determined by the hardware.

8.1 TEST #1, configuration register input/output test

This is the most determinant test because it proves that the chip can be configured. The configuration register is written with random values, keeping the chip always as MASTER and END. The values are then compared with the data returned by the chip in the send identification mode. Since addressing is not meant to be tested here, the universal address is used.

SETTINGS	CHIP configuration	MASTER END SEND_ID_MODE SELECT_0	
	CHIP bias	Ipreamp	220 μ A
		Ishaper	30 μ A
		Threshold DAC	0xFF
	TRIM DAC	Value	0000
		Range	00
CHIP address	Universal address in command		
COMMAND	L1 trigger		
SCANS	LOOPS	1. Random setting of the remaining configuration register bits	
	No. of triggers	100	

Table 6: Configuration register input/output test (digital TEST#1).

8.2 TEST #2, addressing test

The chip is given a random address and is configured using that address. The value is contained in the chip data, it is verified by the usual procedure of comparison with the simulation. Extra tests are done during this procedure: the L1 counter is scanned, the BC counter, the overflow function and the error codes are tested.

SETTINGS	CHIP configuration	MASTER END EDGE_ON DATA_COMPRESSION_01X SEND_ID_MODE SELECT_0	
	CHIP bias	Ipreamp	220 μ A
		Ishaper	30 μ A
		Threshold DAC	0xFF
	TRIM DAC	Value	0000
		Range	00
	CHIP address	Random	
COMMAND	L1 trigger		
SCANS	LOOPS	1. Random setting of address bits 2. L1 Counter scan.	
	No. of triggers	100	

Table 7: Addressing test (digital TEST #2).

8.3 TEST #3, data compression logic

The chip is scanned with different data compression criteria when random masks are applied. Hits are placed in the 1st/2nd/3rd bit of the 3-bit hit description.

SETTINGS	CHIP configuration	MASTER END EDGE_ON DATA_TAKING_MODE SELECT_0	
	CHIP bias	Ipreamp	220 μ A
		Ishaper	30 μ A
		Threshold DAC	0xFF
	TRIM DAC	Value	0000
		Range	00
	CHIP address	Universal address in command	
COMMAND	Set Config. Register + Set Mask Register + Soft Reset + Enable Data Taking Mode + Pulse Input Register + L1 trigger		
SCANS	LOOPS	DCL Mode = { Hit, Level, Edge, Test }	
	No. of triggers	100	

Table 8: DCL test (digital TEST #3).

8.4 TEST #4, dynamic pipeline test

To check the functionality of the mask register and data readout block (pipeline, readout buffer, data compression and LED output), the four (masks #1, #2, #3 and #4) patterns are loaded in the mask register and the input register is pulsed. Pulsing the input register issues one BCO clock pulse to the channels allowed by the mask register.

SETTINGS	CHIP configuration	MASTER END EDGE_ON DATA_COMPRESSION_01X DATA_TAKING_MODE SELECT_0	
	CHIP bias	lpreamp	220 μ A
		Ishaper	30 μ A
		Threshold DAC	0xFF
	TRIM DAC	Value	0000
		Range	00
CHIP address	Universal address in command		
COMMAND	Set Config. Register + Set Mask Register + Soft Reset + Variable (pipeline) Delay + Enable Data Taking Mode + Pulse Input Register + 156 BCO delay + L1 trigger		
SCANS	LOOPS	1. MASK = {mask#1, mask#2,mask#3,mask#4} 2. Pipeline scan	
	No. of triggers	100	

Table 9: Dynamic pipeline test (digital TEST #4).

8.5 TEST #5, token/data passing

The chip is set as a slave and middle chip. During the test the token transmission, as well as passing the data sequence from another slave chip is checked for both lines (0 and 1). Input-bypass and output-bypass bits in the configuration register toggle to realize the four data redundancy scenarios.

SETTINGS	CHIP configuration	SLAVE MIDDLE EDGE_ON DATA_COMPRESSION_X1X DATA_TAKING_MODE SELECT_0	
	CHIP bias	lpreamp	220 μ A
		Ishaper	30 μ A
		Threshold DAC	0xFF
	TRIM DAC	Value	0000
		Range	00
CHIP address	Universal address in command		
COMMAND	External data/token injection		
SCANS	LOOPS	1. { input_bypass, output_bypass } = { 00, 01, 10, 11 }	
	No. of triggers	100	

Table 10: Token/data passing test (digital TEST #5).

8.6 TEST #6, static pipeline test

The mask bit is in the chip, therefore the data expected are defined by the masks applied to the chip. The four masks are applied and the pipeline is scanned.

SETTINGS	CHIP configuration	MASTER END EDGE_OFF DATA_COMPRESSION_X1X MASK DATA_TAKING_MODE SELECT_0	
	CHIP bias	Ipreamp	220 μ A
		Ishaper	30 μ A
		Threshold DAC	0xFF
	TRIM DAC	Value	0000
		Range	00
CHIP address	Programmed = 1		
COMMAND	Set Config. Register + Set Mask Register + Enable Data Taking Mode + SoftReset + Delay + L1 trigger		
SCANS	LOOPS	1. MASK = {mask#1, mask#2,mask#3,mask#4} 2. Pipeline scan	
	No. of triggers	100	

Table 11: Static pipeline test (digital TEST #6).

8.7 TEST #7, com1 test

To verify the functionality of the redundant circuitry, we run the static pipeline test on the com1 line.

SETTINGS	CHIP configuration	MASTER END EDGE_OFF DATA_COMPRESSION_X1X MASK DATA_TAKING_MODE SELECT_1	
	CHIP bias	Ipreamp	220 μ A
		Ishaper	30 μ A
		Threshold DAC	0xFF
	TRIM DAC	Value	0000
		Range	00
CHIP address	Programmed = 1		
COMMAND	Set Config. Register + Set Mask Register + Enable Data Taking Mode + SoftReset + Delay + L1 trigger		
SCANS	LOOPS	1. MASK = {mask#1, mask#2,mask#3,mask#4} 2. Pipeline scan	
	No. of triggers	100	

Table 12: Com1 test (digital TEST #7).

9 I/O signals levels and phases¹

We test the chip signal levels and phases by running test vectors utilizing these signals and varying the conditions. The working range is exceeded when the test vector efficiency is below 100%. Care is taken to minimize signal interference, by employing test vectors with isolated signal usage.

Signal Name	Signal Type	Test Vector Used
CLK0	input	TEST #1
CLK1	input	version of TEST #1 utilizing CLK1/COM1 lines
COM0	input	TEST #1
COM1	input	version of TEST #1 utilizing CLK1/COM1 lines
DATAIN0	input	TEST DAT0 (simple pattern injection for a slave chip)
DATAIN1	input	TEST DAT1 (simple pattern injection for a slave chip)
TOKENIN0	input	TEST #5
TOKENIN1	input	TEST #5
datalink/LED	output	TEST #0 (chip as MASTER & END, do soft reset and trigger, look for the datalink/LED only)
DATAOUT0	output	TEST DAT0 (simple pattern injection for a slave chip)
DATAOUT1	output	TEST DAT1 (simple pattern injection for a slave chip)
TOKENOUT0	output	TEST TOK0 (chip as MASTER & MIDDLE, do soft reset and trigger, look for TOKENOUT0 only)
TOKENOUT1	output	TEST TOK1 (chip as MASTER & MIDDLE, do soft reset and trigger, look for TOKENOUT1 only)

Table 13: Test vectors used to find the level and phase ranges for the input and output signals.

9.1 Input signals levels

The test system uses pin drivers chips with selectable voltage levels to supply the input differential signals to the chip. To test an input signal level, we scan the voltage swing while keeping other signals at the nominal conditions. The minimal voltage swing the system can supply is around 65 mV, which is less than the maximum specified working range of [40, 160 mV] for the DATA and TOKEN input signals. An example histogram is given in Figure 9.

9.2 Output signals levels

The system uses window comparators (WC), which pass the digital signals from the chip only if the high voltage level is above the high WC threshold and the low voltage level is below the low WC level. To find the high and low voltage levels, both WC thresholds are set to the same value, which is varied in the scan. The test vector efficiency is 100% only if the threshold level is between high and low voltage levels. The working range for the differential voltage is [40, 160 mV] for the DATA and TOKEN output signals and it is [250, 400 mV] for the datalink/LED signal. An example histogram is given in Figure 10.

9.3 Input signals phases

Each of the input signals passes through a delay chip. The delay is scanned for a given signal while keeping other signals at nominal conditions. There is an efficiency drop when the rising edge of the clock coincides with the rising edge of the signal inside the chip. The actual delays may be different, and the difference measures the relative signal propagation times in the input circuitries. The width of the sub-100% efficiency region indicates the setup time. The setup time specification is [9, 20 ns] for the COM signals, [0, 15 ns] for the DATAIN signals and [0, 9 ns] for the TOKENIN signals. An example histogram is given in Figure 11.

¹ The tests described in this section are not yet a part of the standard chip validation procedure.

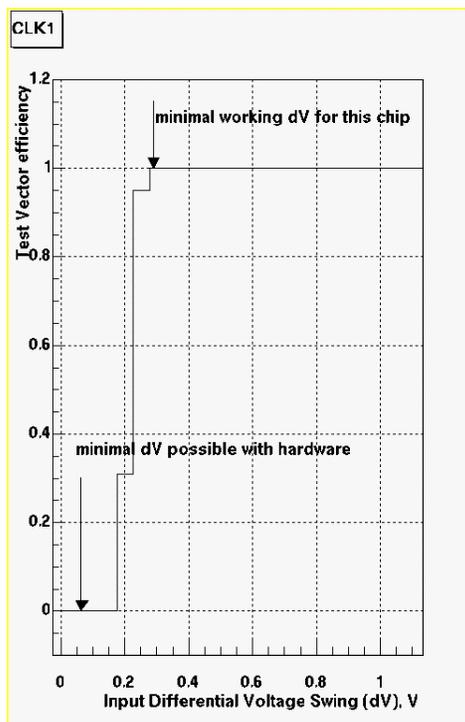


Figure 9: Input voltage scan for CLK1 at 70 MHz.

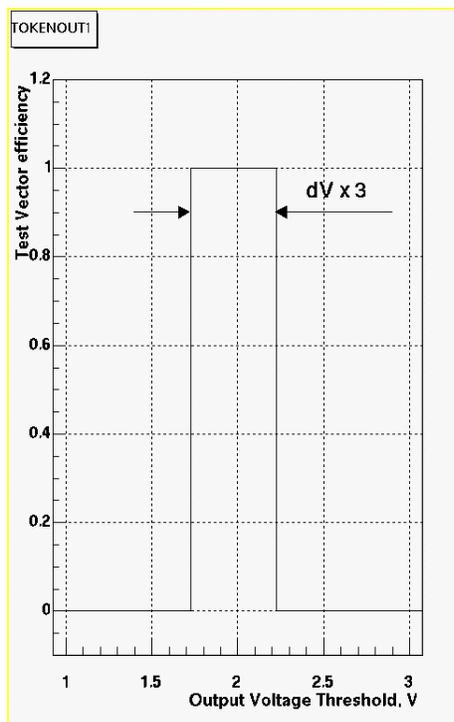


Figure 10: Finding output voltage swing.

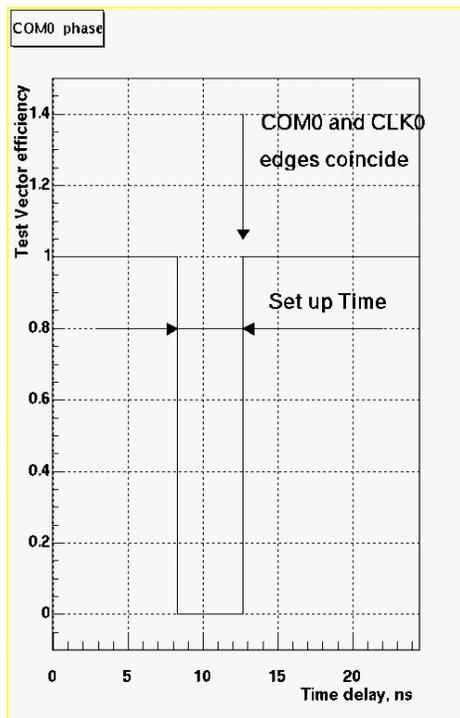


Figure 11: Input phase scan for COM0.

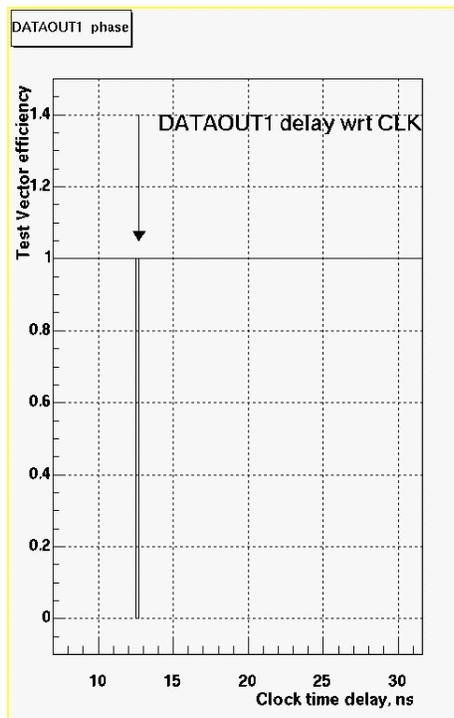


Figure 12: Finding DATAOUT1 phase wrt CLK.

9.4 Output signals phases

All the output signals are passed through a register. We can scan the delay for the clock going to this register to find out the rising edge of a signal by the dip in the efficiency. When running a test vector for a given signal, other output signals are masked off in the data vs. simulation comparison to avoid interference (which may result in multiple dips in the efficiency histogram). For datalink/LED and DATAOUT signal we use the test vectors which does not have other output lines toggling. For TOKENOUT signals we use test vectors which have both datalink/LED and TOKENOUT lines toggling, although only TOKENOUT is being enabled. An example histogram is given in Figure 12. The nominal output signal delay ranges wrt CLK are: [16, 40 ns] for the datalink/LED, [12, 33 ns] for the DATAOUT, and [14.5, 39 ns] for the TOKENOUT.

9.5 Clock duty cycles

We use the delay chips for the clocks to scan their duty cycle. The test system is capable of changing the duty cycle in the range of [0.35, 0.8]. We require that the corresponding test vector efficiency is 100% in the region [0.4,0.6] at 40 MHz (Figure 15).

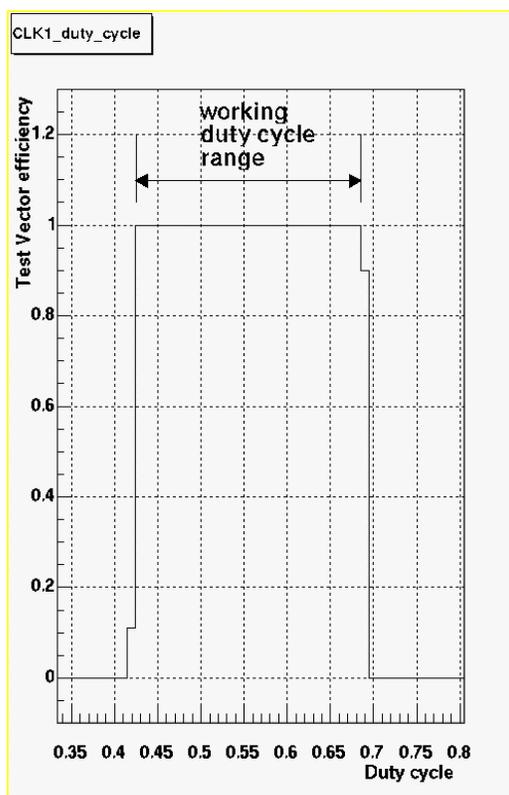


Figure 15: The scan of CLK1 duty cycle taken at 60 MHz.

10 Flow of data

Results of all tests together with the chip coordinates on the wafer are saved on HD. One file per chip is created during the screening. Raw data from the whole wafer is analyzed using the ROOT package. One root file is created for the whole wafer. It contains many predefined histograms with the parameters extracted from the scans. Information about the position on the wafer, chip performance, wafer and batch reference is stored in this file. The root files are used to extract the information for user database and to produce the bin files used in yield analysis. The flow of data is shown in Figure 16.

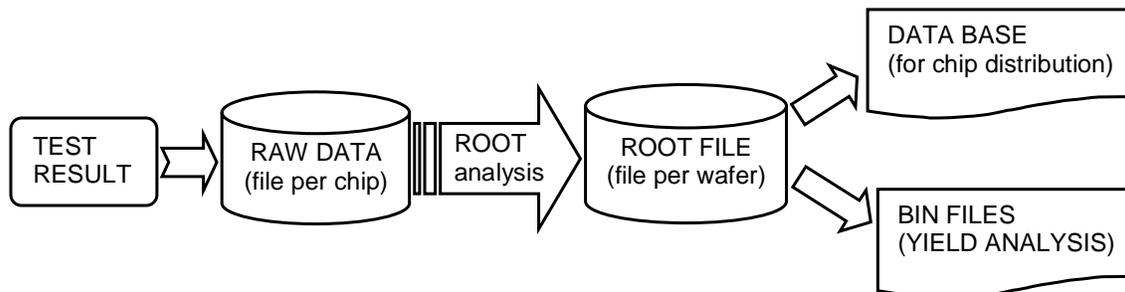


Figure 16: Flow of data extracted from the screened wafers with the ABCD3T chips.

10.1 Format of the ROOT file

As mentioned above the raw data is processed and the information compiled using the ROOT packages into so-called *root files*. ROOT is a general purpose C++ package for data manipulation [5]. The environment created with ROOT for the wafer screening setup follows a hierarchical architecture, as data does. Four classes are defined: Wafer, Chip, Channel and ScanPoint. They reflect how the data are organised: A wafer has chips with a number of channels on which we perform a number of tests: the points in a scan of some of their parameters. In the root file, every class is stored in a sort of list, a Ttree in the ROOT jargon. The Wafer tree contains the Wafer class, which knows about the number of chips it contains and where they are located in the Chip Ttree. The same occurs with the Channel Ttree w.r.t the Chip Ttree and the ScanPoint Ttree w.r.t the Channel Ttree. On top of that, every class contains all the information of the screening configuration. The Chip class will contain information about the bias, digital test performed on it, etc, while a channel will contain information about which parameters have been scanned and over which range. A ScanPoint class will contain the information of the actual values of the scan point for a channel. Also every class is able to produce summaries about any parameter of the classes below it in the hierarchical tree. For instance the Chip class will be able to survey the noise of the channels for any of the scan points, that is, for any input calibration pulse. More detailed information about these files can be found in the description of the software [3].

This structure of the data eases the analysis and reduction of the information. It helps in preparing the data in all the formats needed in further steps of the testing process like building the database for chip distribution or the data files needed by the vendor for the yield analysis.

10.2 Definition of BIN and yield analysis

As was mentioned at the beginning of this document, the described system for wafer screening should provide input for the yield analysis of the ABCD3T chips. The basis for the yield analysis is the bin file. The format of the bin file is accepted by the ATMEL foundry and it allows bin analysis to control and possibly improve the yield during the production of the ABCD3T chips. A chip can obtain only one bin number, which is the result of all tests performed on this die (to be compatible with the software used in ATMEL allowing for yield analysis). The definitions of the bins include all pass/fail criteria for the ABCD3T chips (bin 0 – chip accepted etc.). The result of the digital test is taken for a given value of power supply and frequency. This value is set in the flat region of the yield versus Vdd figure (see figure 3). For batches Z29476, Z30423 and Z31122, Vdd = 3.8V and a frequency of 50MHz were used as threshold parameters for the digital tests. Definition of the bins is shown in table 14. The ROOT macro used for the production of the bin files is described in the document [3].

Assignment of only a single bin to each chip compresses the information available from the root file. It allows for a simple correlation analysis to be performed between the bin files and the results of the process control monitoring test structures and map of defects performed at ATMEL. The sequence in which we define the bin for a given chip is important and may influence the eventual location of the defects on the chip. The algorithm for assigning bins to chips is shown in figure 17. Two types of the bin files are produced during the test analysis. Type “1” bin file comprising the list of the chips and their coordinates on the wafer and the bin result (one bin

file per wafer). Type “2” bin file contains the list of the wafers for a given batch with the summary of bins for each wafer (one bin file per batch).

BIN	DEFINITION
0	Good chip (after all tests)
2	failed DIGITAL TEST#1 (Config Reg.) @ 3.8V & 50MHz
3	failed DIGITAL TEST#2 (Addressing) @ 3.8V & 50MHz
4	failed DIGITAL TEST#3 (DCL) @ 3.8V & 50MHz
5	failed DIGITAL TEST#6 (Static pipeline) @ 3.8V & 50MHz
6	failed DIGITAL TEST#5 (token/data passing) @ 3.8V & 50MHz
7	failed DIGITAL TEST#4 (dynamic pipeline) @ 3.8V & 50MHz
8	failed DIGITAL TEST#7 (com1 test) @ 3.8V & 50MHz
9	defect(s) in analog part #2 (channel offset out of the Trim DAC range 1 or discrepancy between gain and average gain higher than 25% or channel noise is 3 times higher than average noise of the chip or discrepancy between average gain of the chip and average gain from the wafer is higher than 30%)
10	defect(s) in analog part #1 (no response to the calibration pulses)
11	between 1 to 10 defects in the pipeline (low analog efficiency)
12]10-100] defects in the pipeline (low analog efficiency)
13	> 100 defects in the pipeline (low analog efficiency)
14	high power consumption in digital part (Slave mode) (> 30% average ²)
15	high power consumption in analog part (Slave mode) (> 30% average)
16	low power consumption in digital part (Slave mode) (<30% average)
17	low power consumption in analog part (Slave mode) (<30% average)
18	Non-linear Threshold DAC (MAX ERR>10%)
19	Non-linear Bias1 (Preamp) DAC (MAX ERR>25%)
20	Non-linear Bias2 (Shaper) DAC (MAX ERR>25%)
21	Defect in the TRIM DAC (MAX ERR>25% or discrepancy between Trim DAC range 0 for a given channel and TrDACRange0 is higher than 40%)
22	Defect in Trim DAC ranges (discrepancies between TrDACRange0 + TrDACRange3 and averages from the wafer are higher than 40%)
23	Chip noise is outside of wafer noise distribution
24	Strict digital test failed at Vdd = 3.8 and 40MHz
25	Strict digital test failed at Vdd = 3.8 and 50MHz
26	Calibration line failure pattern on gain vs. channel data
27	Calibration line failure pattern on offset vs. channel data
28	S-curve points have more than 1.0 efficiency (DCL problem) (implemented, but not enabled yet)

Table 14: Definition of the bins

² Average of power consumption is calculated from the ABCD chips passing the digital tests (bins 2 ÷ 8).

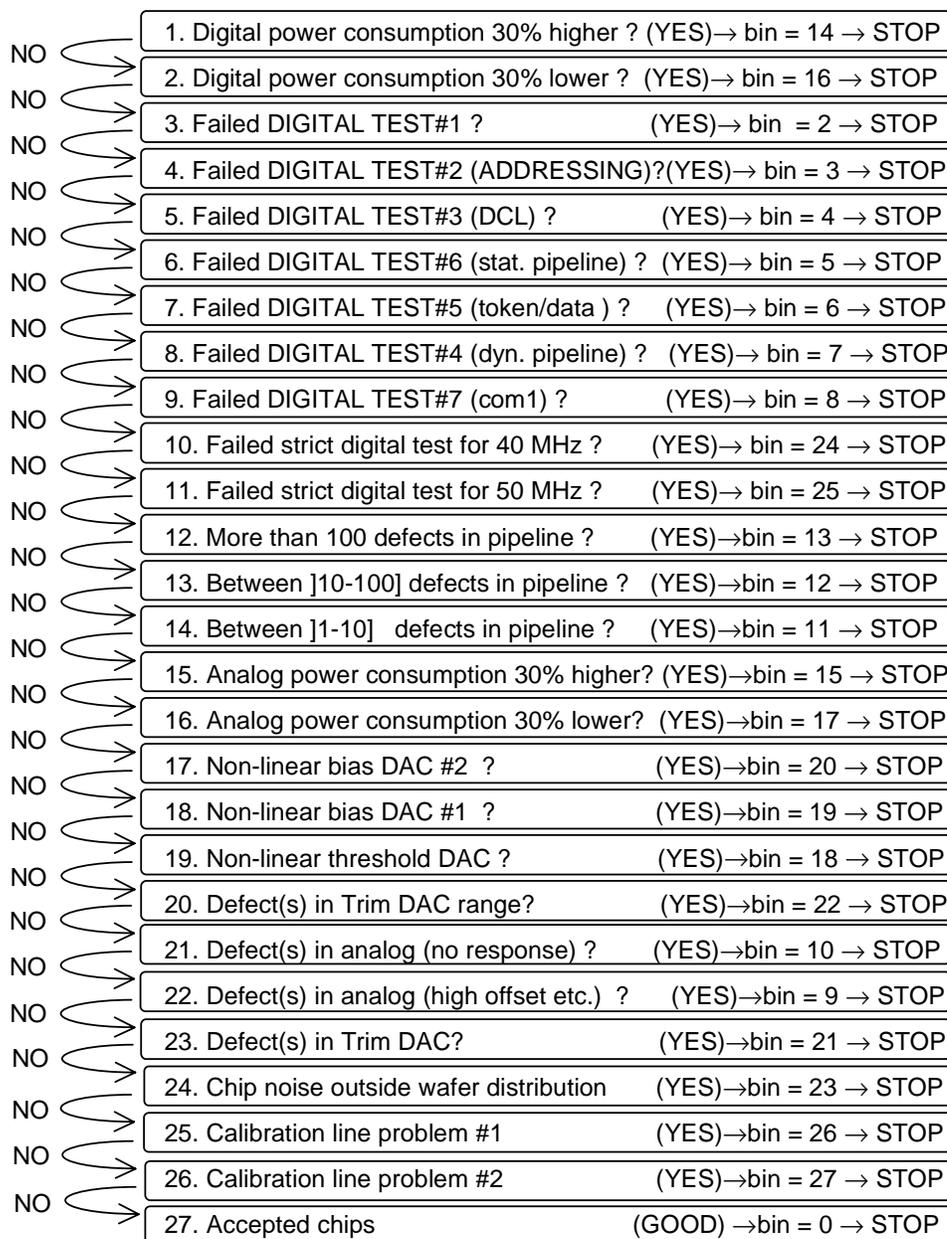


Figure17: Algorithm for binning the test results.

An extra cross check is used when we look for the defects in the pipeline not detected by the digital TEST#4 and TEST#6. Because of the multiplexed structure, defects in the pipeline affect the efficiency of the analogue scans. Looking at the efficiency of the S-curves obtained during the threshold scans, one can find defects in the pipeline. In this way a bins with number 10, 11 and 12 are obtained. The examples of the bin files are shown in figure 18a and 18b.

```

[BEGIN OF FILE]
Z31122,990T,06,6,20,14
Z31122,990T,06,5,20,10
.
.
Z31122,990T,06,4,19,0
Z31122,990T,06,3,19,6
Z31122,990T,06,7,18,14
Z31122,990T,06,6,18,5
[END OF FILE]

```

Figure 18a: Example of bin file type 1 for wafer 6, batch31122

```

Z31122,990T,2,35,0,3,0,1,32,28,0,1,1,11,2,0,0,13,1,0,0,0,0,0,0,,
Z31122,990T,3,47,0,6,0,0,17,12,0,1,2,24,3,0,0,15,1,0,0,0,0,0,0,,
Z31122,990T,4,55,0,5,0,1,24,7,1,0,1,13,3,1,0,14,1,0,1,1,0,0,0,0,,
Z31122,990T,5,49,0,4,0,1,21,16,0,0,1,15,1,1,0,17,1,0,1,0,0,0,0,0,,
Z31122,990T,6,53,0,2,0,0,26,18,0,0,2,13,0,0,0,12,2,0,0,0,0,0,0,0,,
Z31122,990T,8,43,0,2,0,2,24,7,0,0,4,26,5,2,0,12,0,0,1,0,0,0,0,0,,
Z31122,990T,9,46,0,4,0,2,18,16,0,0,2,26,3,0,0,10,1,0,0,0,0,0,0,0,,
Z31122,990T,10,69,0,1,0,2,17,10,0,0,2,16,1,0,0,10,0,0,0,0,0,0,0,0,,
Z31122,990T,11,43,0,1,0,1,27,10,0,0,2,25,2,0,0,15,1,0,1,0,0,0,0,0,,
Z31122,990T,,48,0,3,0,1,22,13,0,0,1,18,2,0,0,13,0,0,0,0,0,0,0,0,9,

```

Figure 18b: Example of summary bin file for batch Z31122 (type 2)

The different parameters in the first line of figure 18a mean:

```

Z31122 : Lot number
990T   : ATMEL reference probe step
06,    : Wafer number
6,20   : Chip X,Y position
14     : Bin Results

```

The different parameters in the first line of figure 18b mean:

```

Z31122 : Lot number
990T   : ATMEL reference probe step
2      : Wafer number
35     : sum of die with the bin number 0 (ie; the sum of good die)
0      : sum of die with the bin number 1
3      : sum of die with the bin number 2
.
.
.

```

In this file a comma is placed at the end of each line.

The last line of this file contains the following information:

```

Z31122 : Lot number
990T   : Our reference probe step
,      : no reference wafer number: comma is placeholder
48     : average of the first bin of the lot (bin number 0)
0      : average of the second bin of the lot (bin number 1)
0      : average of the third bin of the lot (bin number 3)

```

The last parameter (9) is the number of wafer in the batch.

The summary bin file shows a distribution of the defects in different blocks of the chip and gives to the particular batch a kind of signature which may be used for comparison between different production lots. The summary bin file is also a basis for yield analysis. Making a simple calculation we can easily define the yield in different parts of the chip (yield in analogue part of the chip, yield in digital part of the chip and final yield for the whole die). Summing all the bins one can get the total number of dies (SUM). The number of good dies (GOOD) is the number of dies with the bin 0. Summing the dies with the bins from 2 to 8 and bins 11,12,13,14 and 16 we will get the number of dies with defects in the digital part of the chip (DIG_DEFECTS). Summing the chips tagging with the bins number 15, 17, 20, 19, 10, 9, 18, 21 and 22 we will get the number of chips with defects in the analogue part of the chip (AN_DEFECTS).

Then the yield can be defined as:

- Final yield [%] = 100 * GOOD / SUM
- Digital yield [%] = 100 * (SUM – DIG_DEFECTS) / SUM
- Analogue yield [%] = 100 * (SUM – DIG_DEFECTS – AN_DEFECTS) / (SUM – DIG_DEFECTS)

The yield results for the analysed batch Z31122 using described formulas is shown in Figure 19.

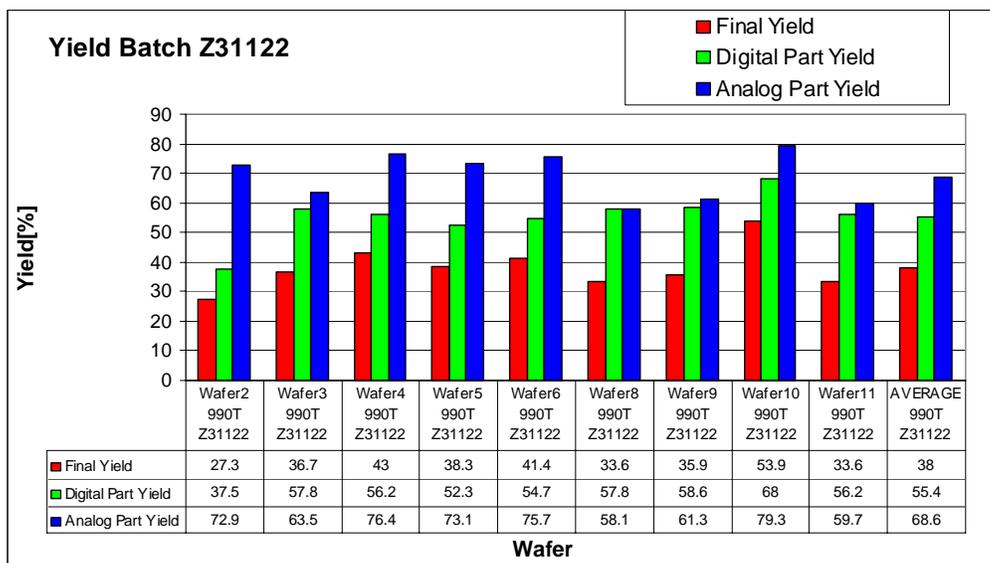


Figure 19: Yield results from batch Z31122 manufactured in March 2000.

10.3 Parameters transferred to the ACCESS user database

The user database allows for distribution of the chips with a requested quality to the clients. Selection and distribution of the chips will be done based only on the chip parameters written in the database. Thus it is necessary to provide a complete list of the parameters describing the performance of the chips and their properties. The list of parameters extracted from all tests and describing the status of the chip (used, not used, destination place), batch, wafer, wafer coordinates etc. is shown in Table 15. The Microsoft Access database has been used successfully during the preproduction of the ABCD chip. The ATLAS SCT database will be used instead for the production.

WfID	wafer ID (wafer number)
Wftype	wafer type (ABCD2T or ABCD2NT chips)
batch	batch number (for example Z31122)
x,y	chip position on the wafer
digflg	digital flag - for digitally perfect chips equal to 1
Vdd0	minimum Vdd [V] for which chip is fully efficient for all digital tests @ 50MHz
VddCnf0	minimum Vdd [V] for digital TEST#1 @ 50MHz
VddAddr0	minimum Vdd [V] for digital TEST#2 (ADDRESSING) @ 50MHz
VddL1C0	minimum Vdd [V] for digital TEST#2 (L1 counter) @ 50MHz
VddInpReg0	minimum Vdd [V] for digital TEST#3 @ 50MHz
VddInpLin0	minimum Vdd [V] for digital TEST#4 (MASK) @ 50MHz
VddFakeS0	minimum Vdd [V] for digital TEST#5 @ 50MHz
VddSlave0	minimum Vdd [V] for digital TEST#6 @ 50MHz
VddToken0	Minimum Vdd[V] for digital TEST#4 (TOKEN) @ 50MHz
Vdd1	minimum Vdd[V] for which chip is fully efficient for all digital tests @ 40MHz
VddCnf1	same test as VddCnf0 @ 40MHz
VddAddr1	same test as VddAddr0 @ 40MHz
VddL1C1	same test as VddL1C0 @ 40MHz
VddInpReg1	same test as VddInpReg0 @ 40MHz
VddInpLin1	same test as VddInpLin0 @ 40MHz
VddFakeS1	same test as VddFakeS0 @ 40MHz
VddSlave1	same test as VddSlave0 @ 40MHz
VddToken1	same test as VddToken0 @ 40MHz
ThrsDAC	maximum non-linearity error for Threshold DAC ((MAX.ERROR/RANGE))

PreamDAC	maximum non-linearity error for Preamplifier bias DAC ([MAX.ERROR/RANGE])
ShaperDAC	maximum non-linearity error for Shaper bias DAC ([MAX.ERROR/RANGE])
mdigc	power consumption (current) of the digital part in MASTER mode [A]
sdigc	power consumption (current) of the digital part in SLAVE mode [A]
manac	power consumption (current) of the analogue part in MASTER mode [A]
sanac	power consumption (current) of the analogue part in SLAVE mode [A]
ndead	number of dead channels (channels with defects in analogue part)
nontrim	number of channels with non monotonic TRIM DAC characteristic
gain	average gain of the chip [mV/fC]
sgain	sigma deviation of the channel gains on the chip [mV/fC]
offset	average offset of the chip [mV]
soffset	sigma deviation of the channel offsets on the chip [mV]
qfactor	quality factor defined as: $gain/\sqrt{soffset^2+sgain^2}$
xeff	number of channels with low analogue efficiency (channel with low analogue efficiency is considered as a dead channel also)
dest	destination
date	date of last modification
used	0 – chip available, 1 – chip used
comments	no comments

Table 15: List of the fields in the ACCESS database.

10.4 Parameters transferred to ATLAS SCT database

For proper managing of the ABCD3T chips during the production, screening and assembling of the modules an official ATLAS SCT database is used. The list of the parameters extracted from the wafer screening transferred to that database is listed in table 15,16 and 17. All fields are mandatory.

ITEM/CHIP unit	
MFR_SER_NO	BATCH-WAFER-XPOS-YPOS (example Z34685-W01-X05-Y05) – manufacturer serial number consist of number of batch, wafer number and x,y position of chip on the wafer
RECEIPT_DATE	Date of reception of material (wafers)
LOCATION	Location of the material (for example CERN)

Table 16: List of parameters transferred to the SCT database for the ITEM/ABCD article.

Together with the status of the chip (location, serial number, manufacturer serial number etc.) described in table 17 a set of parameters describing results of the screening tests are loaded into the database. A test data structure for the ABCD3T chips after wafer screening consist of two entities. The TEST_ABCD article is a set of parameters extracted for the whole chip like average gain, noise, results of digital tests etc. The TESTABCDCHANNELS entity related to a given ABCD3T chip describes parameters of the single channel (gain, noise etc.) for a given channel number which is a primary key for that article. Beside of screening results, the wafer electrical parameters based on electrical test structures delivered by ATMEL are also stored into database. There are 5 sets of these structures on each wafer. The WAFER_E_PARAM table describes the most important ones. Type and range of passed parameters are described in appendix A.

TEST_ABCD unit	
MachineName	Name of the machine used for wafer screening
OnlineSoftRev	On-line software revision
OfflineSoftRev	Off-line software revision
PreampBias	Value of bias for the preamplifier stage used in the test [uA]
ShaperBias	Value of bias for the shaper stage used in the test [uA]
PrfFlg	Perfect flag – for absolutely perfect chips (depends on software revision and update)
DigFlg	Digital flag - for digitally perfect chips equal to 1
DppFlg	Digital Perfect Pattern flag (internal use)
Vdd0	Minimum Vdd [V] for which the chip is fully efficient for all digital tests @ 50MHz

Vdd0strict	Minimum Vdd [V] for which the chip is fully efficient for all STRICT digital tests @ 50MHz
VddTest1F0	Minimum Vdd [V] for digital TEST vector #1 @ 50MHz
VddTest2F0	Minimum Vdd [V] for digital TEST vector #2 @ 50MHz (old system: Minimum Vdd [V] for digital TEST#2 (ADDRESSING) @ 50MHz)
VddTest3F0	Minimum Vdd [V] for digital TEST vector #3 @ 50MHz (old system: Minimum Vdd [V] for digital TEST#2 (L1 counter) @ 50MHz)
VddTest4F0	Minimum Vdd [V] for digital TEST vector #4 @ 50MHz (old system: Minimum Vdd [V] for digital TEST#3 @ 50MHz)
VddTest5F0	Minimum Vdd [V] for digital TEST vector #5 @ 50MHz (old system: Minimum Vdd [V] for digital TEST#4 (MASK) @ 50MHz)
VddTest6F0	Minimum Vdd [V] for digital TEST vector #6 (old system: Minimum Vdd [V] for digital TEST#5 @50MHz)
VddTest7F0	Minimum Vdd [V] for digital TEST vector #7 (old system: Minimum Vdd [V] for digital TEST#6 @50MHz)
Vdd1	Minimum Vdd[V] for which the chip is fully efficient for all digital tests @ 40MHz
Vdd1strict	Minimum Vdd[V] for which the chip is fully efficient for all STRICT digital tests @ 40MHz
VddTest1F1	Same test as VddTest1F0 @ 40MHz
VddTest2F1	Same test as VddTest2F0 @ 40MHz
VddTest3F1	Same test as VddTest3F0 @ 40MHz
VddTest4F1	Same test as VddTest4F0 @ 40MHz
VddTest5F1	Same test as VddTest5F0 @ 40MHz
VddTest6F1	Same test as VddTest6F0 @ 40MHz
VddTest7F1	Same test as VddTest7F0 @ 40MHz
ThrsDACsSlope	Threshold DAC slope [mV/bit] obtained from linear fit to the measurement points.
ThrsDACErr	Maximum non-linearity error for Threshold DAC (maximum dispersion of the measurement point from the linear fit [mV])
PreampDACsSlope	Preamplifier bias DAC slope [mV/bit] obtained from linear fit to the measurement points (direct values in mV readout from the probe pad – for the conversion to uA refer to section 7).
PreamDACErr	Maximum non-linearity error for Preamplifier bias DAC (maximum dispersion of the measurement point from the linear fit [mV])
ShaperDACsSlope	Shaper bias DAC slope [mV/bit] obtained from linear fit to the measurement points (direct values in mV readout from the probe pad – for the conversion to uA refer to section 7).
ShaperDACErr	Maximum non-linearity error for Shaper bias DAC (maximum dispersion of the measurement point from the linear fit [mV])
MDigC	Power consumption (current) of the digital part in MASTER mode [A]
SDigC	Power consumption (current) of the digital part in SLAVE mode [A]
MAnaC	Power consumption (current) of the analogue part in MASTER mode [A]
SAnaC	Power consumption (current) of the analogue part in SLAVE mode [A]

NdNoResp	Number of channels not responding to calibration pulses (bin10)
NdPipeline	Number of channels with low analogue efficiency (pipeline defects)
NdNoise	Number of noisy channels (bin 9)
NdGain	Number of channels with degraded gain (bin9)
NdTrim	Number of channels with defects in TRIM DACs. Defects in the Trim DACs are verified for range 0 (data available for all channels of the chip). Conditions for verification are the same as for calculation of bin number 21.
NdHOffset0	Number of channels with offset out of the Trim DAC range 0
NdHOffset1	Number of channels with offset out of the Trim DAC range 1 (bin 9)
NdHOffset2	Number of channels with offset out of the Trim DAC range 2
NdHOffset3	Number of channels with offset out of the Trim DAC range 3
Ndead	Total number of unusable channels (channels with defects in analogue part).
Status	BIN status of the chip
StatusValid	Validation word for Status
AuxFlags	Auxiliary flags
AvGain	Average gain of the chip [mV/fC]
SGain	Sigma deviation of the channel gains on the chip [mV/fC]
MaxGain	Maximum channel gain in the chip [mV/fC]
MinGain	Minimum channel gain in the chip [mV/fC]
AvOffset	Average offset of the chip [mV]
SOffset	Sigma deviation of the channel offsets on the chip [mV]
MaxOffset	Maximum channel offset in the chip [mV]
MinOffset	Minimum channel offset in the chip [mV]
MaxTrDACErr	Maximum nonlinearity error for Trim DAC range 0 [mV]
MaxTrSlope	Maximum Trim DAC slope [mV/bit] of the Trim DAC characteristic (Range 0)
MinTrSlope	Minimum Trim DAC slope [mV/bit] of the Trim DAC characteristic (range 0)
TrDACRange0	Average of the ranges 0 of the trim DACs in the chip [mV]
TrDACRange1	Average of the ranges 1 of the trim DACs in the chip [mV]
TrDACRange2	Average of the ranges 2 of the trim DACs in the chip [mV]
TrDACRange3	Average of the ranges 3 of the trim DACs in the chip [mV]
AvNoise	Average output noise of the chip [mV] (extracted from point #1)
SNoise	Sigma deviation of the channel output noise on the chip [mV] (point #1)
MaxNoise	Maximum channel output noise in the chip [mV] (point #1)
MinNoise	Minimum channel output noise in the chip [mV] (point #1)
Qfactor	Quality factor defined as: $\text{gain}/\text{SQRT}(\text{soffset}^2 + \text{sgain}^2)$
Bin	Result of bin analysis (number from 0 to 28)

Table 17: List of parameters transferred to the SCT database for the TEST_ABCD article.

TSTABCDCHANNELS unit	
Chann_number	Channel number – primary key for this table
Gain	Gain for a given channel [mV/fC]
Offset	Offset for a given channel [mV]
Noise	Output noise for a given channel [mV]
TrDACsSlope	Slope of the Trim DAC characteristic (Range 0) in [mV/bit]

TrDACErr	Maximum non-linearity error for Trim DAC (maximum dispersion of the measurement point from the linear fit [mV]) for Range 0
ChStatus	BIN status of channel

Table 18: List of the parameters transferred to the SCT database for the TSTABCDCHANNELS entity.

WAFER_E_PARAM unit	
STRUCTURE	test structure number [no unit]
VTN08	nmos threshold voltage [V]
IDN08	nmos (25u/0.8u with Vgs=Vds=5V) drain current [mA]
BVN08	nmos breakdown voltage [V]
VTP08	pmos threshold voltage [V]
IDP08	pmos (25u/0.8u with Vgs=Vds=5V) drain current [mA]
RSBL	N-well/N+ buried layer sheet resistance [ohm/square]
RSN_PLUS	n+ sheet resistance [ohm/square]
RSP_PLUS	p+ sheet resistance [ohm/square]
RSP1	silicided poly sheet resistance [ohm/square]
BETA_AT_10	forward gain of 1.2um x 1.2um NPN with Ic=10uA and collector biased at 2.0V (at room temp.) [nounit]
BETA_AT_100	forward gain of 1.2um x 1.2um NPN with Ic=100uA and collector biased at 2.0V (at room temp.) [nounit]
VAT	early voltage of 1.2um x 1.2um NPN with base tied to 0.7V, emitter grounded [V]
BVCEOT	breakdown of collector-emitter junction with base open [V]
BVCEST	breakdown of collector-emitter junction with base grounded [V]
VPPJ12	pinch-off voltage of a 100/1.2 P-channel JFET [V]
IDPJ12	drain current of a 100/1.2 P-channel JFET at Vgs=0, Vds= -5V [uA/um]
RCM1N_PLUS	contact resistance between M1 and N+ [ohms/contact]
RCM1P_PLUS	contact resistance between M1 and P+ [ohms/contact]
RCM1P1	contact resistance between M1 and silicided poly [ohms/contact]
RCM2M1	contact resistance between M1 and M2 [ohms/contact]
RSRHV	“high value” resistance of the resistor object [kohms/c]
Rextrins	no def [kohm/c]
TOXP1N_PLUS	gate oxide thickness over nmos [Angstrom]
B12x10_AT_10	beta no def [nounit]
B12x10_AT_100	beta no def [nounit]
VEARLY	early voltage [V]
CP1TOX	gate oxide capacitance [aF/um^2]
CP1HOX	gate oxide capacitance over vtcapa implant [af/um^2]

Table 19: List of the parameters transferred to the SCT database for the WAFER_E_PARAM entity.

10.5 Procedures for filling the SCT database with the wafer screening results.

- Uploading the chips to the database is done via a java application provided by the manager of the database
- The encoding scheme for ITEMS.mfr_ser_no will be kept as a function of wafer_ser_no, XChipcoordinate, YChipcoordinate
- Since the primary key of ITEMS is based only on the ITEMS.ser_no and no more constraints will be added to the ITEMS table, the application will be responsible for informing the user that the chips have not already been inserted into the database. The application will do that by checking the unique state of the ITEMS.MFR_SER_NO attribute before inserting the item chip.
- An optional function to populate the SHIPS and SHIP_ITEMS automatically during the chips registration will also be implemented in this new java application. A special report will be developed to allow the users to make a shipment of a set of selected chips. The criteria for selecting the chips will be defined in future.

- The report will give the possibility to automatically populate the ships and ship_items tables with the record set by the criteria.
- The web application already allow the users who are the owner of the shipped items and shipments to delete or update ITEMS, SHIPS and SHIP_ITEMS records.
- When all the ship_items have been inserted (using the java application or the Web interface or else), the user is able “to send” (from a database point of view) the items to the destination person and institute, by updating the “Send Confirmation Date” field of the current shipment using his web browser.

11 Appendix A

Definitions for SCT production database for items described in sec. 10.4. **All fields are mandatory, range inclusive** for tables: **ITEM/CHIP, TEST_ABCD, TESTABCDCHANNELS**. For table **WAFER_E_PARAM** all fields **optional** except **STRUCTURE**. Warning and error ranges are inclusive. If parameter is outside warning range database upload process should generate warning message.

ITEM/CHIP unit	TYPE	Range
MFR_SER_NO	STRING(32)	no range
RECEIPT_DATE	DATE	no range
LOCATION	STRING(32)	no range

Table A.1 Definition of type and ranges for ITEM/CHIP unit

TEST_ABCD unit	TYPE	Range
MachineName	STRING(32)	no range
OnlineSoftRev	STRING(16)	no range
OfflineSoftRev	STRING(16)	no range
PreampBias	FLOAT	[0.0,500.0]
ShaperBias	FLOAT	[0.0,500.0]
Prfflg	BOOLEAN	True/False
DigFlg	BOOLEAN	True/False
dpp	BOOLEAN	True/False
Vdd0	FLOAT	[3.3,4.5]
Vdd0strict	FLOAT	[3.3,4.5]
VddTest1F0	FLOAT	[3.3,4.5]
VddTest2F0	FLOAT	[3.3,4.5]
VddTest3F0	FLOAT	[3.3,4.5]
VddTest4F0	FLOAT	[3.3,4.5]
VddTest5F0	FLOAT	[3.3,4.5]
VddTest6F0	FLOAT	[3.3,4.5]
VddTest7F0	FLOAT	[3.3,4.5]
Vdd1	FLOAT	[3.3,4.5]
Vdd1strict	FLOAT	[3.3,4.5]
VddTest1F1	FLOAT	[3.3,4.5]
VddTest2F1	FLOAT	[3.3,4.5]
VddTest3F1	FLOAT	[3.3,4.5]
VddTest4F1	FLOAT	[3.3,4.5]
VddTest5F1	FLOAT	[3.3,4.5]
VddTest6F1	FLOAT	[3.3,4.5]
VddTest7F1	FLOAT	[3.3,4.5]
ThrsDACsSlope	FLOAT	[0.0,3.125]
ThrsDACErr	FLOAT	[0.0,800.0]
PreampDACsSlope	FLOAT	[0.0,2.0]
PreampDACErr	FLOAT	[0.0,300.0]
ShaperDACsSlope	FLOAT	[0.0,2.0]
ShaperDACErr	FLOAT	[0.0,300.0]
MDigC	FLOAT	[0.0,0.2]
SDigC	FLOAT	[0.0,0.2]
MAnaC	FLOAT	[0.0,0.2]
SAnaC	FLOAT	[0.0,0.2]
NdNoResp	BYTE	[0,128]
NdPipeline	BYTE	[0,128]
NdNoise	BYTE	[0,128]

NdGain	BYTE	[0,128]
NdTrim	BYTE	[0,128]
NdHOffset0	BYTE	[0,128]
NdHOffset1	BYTE	[0,128]
NdHOffset2	BYTE	[0,128]
NdHOffset3	BYTE	[0,128]
Ndead	BYTE	[0,128]
Status	UNSIGNED LONG (32bit) bit accessible	[0,4294967295]
StatusValid	UNSIGNED LONG (32bit) bit accessible	[0,4294967295]
AuxFlags	UNSIGNED LONG (32bit) bit accessible	[0,4294967295]
AvGain	FLOAT	[0.0,500.0]
SGain	FLOAT	[0.0,50.0]
MaxGain	FLOAT	[0.0,500.0]
MinGain	FLOAT	[0.0,500.0]
AvOffset	FLOAT	[-600.0,600.0]
SOffset	FLOAT	[0.0,400.0]
MaxOffset	FLOAT	[-600.0,600.0]
MinOffset	FLOAT	[-600.0,600.0]
MaxTrDACErr	FLOAT	[0.0,100.0]
MaxTrSlope	FLOAT	[0.0,10.0]
MinTrSlope	FLOAT	[0.0,10.0]
TrDACRange0	FLOAT	[0.0,500.0]
TrDACRange1	FLOAT	[0.0,500.0]
TrDACRange2	FLOAT	[0.0,500.0]
TrDACRange3	FLOAT	[0.0,500.0]
AvNoise	FLOAT	[0.0,50.0]
SNoise	FLOAT	[0.0,50.0]
MaxNoise	FLOAT	[0.0,50.0]
MinNoise	FLOAT	[0.0,50.0]
Qfactor	FLOAT	[0.0,20.0]
Bin	BYTE	[0,28]

Table A.2 Definition of type and ranges for TEST_ABCD unit

TSTABCDCHANNELS unit	Type	Range
Chann_number	BYTE	[0,127]
Gain	FLOAT	[0.0,500.0]
Offset	FLOAT	[-600.0,600.0]
Noise	FLOAT	[0.0,50.0]
TrDACsSlope	FLOAT	[0.0,10.0]
TrDACErr	FLOAT	[0.0,100.0]
ChStatus	UNSIGNED LONG (32bit) bit accessible	[0,4294967295]
ChStatusValid	UNSIGNED LONG (32bit) bit accessible	[0,4294967295]

Table A.3 Definition of type and ranges for TSTABCDCHANNELS unit

WAFER_E_PARAM unit	type	error range	warning range
Structure	BYTE	[1,5]	[1,5]
VTN08	FLOAT	[0.0,5.0]	[0.730,1.130]
IDN08	FLOAT	[0.0,20.0]	[6.780,10.290]
BVN08	FLOAT	[0.0,25.0]	[8.000,17.780]
VTP08	FLOAT	[0.0,5.0]	[0.600,1.000]
IDP08	FLOAT	[0.0,20.0]	[3.850,5.900]
BVP08	FLOAT	[0.0,20.0]	[10.0,16.170]
RSBL	FLOAT	[0.0,1000.0]	[405.0,635.0]
RSN_PLUS	FLOAT	[0.0,200.0]	[48.0,72.0]
RSP_PLUS	FLOAT	[0.0,200.0]	[90.0,146.0]
RSP1	FLOAT	[0.0,5.0]	[2.000,2.700]
BETA_AT_10	FLOAT	[0.0,1000.0]	[120.0,350.0]
BETA_AT_100	FLOAT	[0.0,1000.0]	[120.0,350.0]
VAT	FLOAT	[0.0,500.0]	[80.0,190.0]
BVCEOT	FLOAT	[0.0,20.0]	[5.5,15.0]
BVCEST	FLOAT	[0.0,30.0]	[8.0,18.050]
VPJ12	FLOAT	[0.0,5.0]	[8.0,1.8]
IDPJ12	FLOAT	[0.0,50.0]	[7.0,25.0]
RCM1N_PLUS	FLOAT	[0.0,100.0]	[0.0,30.0]
RCM1P_PLUS	FLOAT	[0.0,200.0]	[0.0,80.0]
RCM1P1	FLOAT	[0.0,2.0]	[0.0,0.9]
RCM2M1	FLOAT	[0.0,1.0]	[0.0,0.5]
RSRHV	FLOAT	[0.0,10.0]	[2.5,4.6]
Rextrins	FLOAT	[0.0,10.0]	[1.6,2.3]
TOXP1N_PLUS	FLOAT	[0.0,1000.0]	[370.0,470.0]
B12x10_AT_10	FLOAT	[0.0,1000.0]	[120.0,350.0]
B12x10_AT_100	FLOAT	[0.0,1000.0]	[120.0,350.0]
VEARLY	FLOAT	[0.0,250.0]	[35.0,150.0]
CP1TOX	FLOAT	[500.0,3000.0]	[1816.0,2156.0]
CP1HOX	FLOAT	[500.0,1500.0]	[767.0,986.0]

Table A.4 Definition of type and ranges for WAFER_E_PARAM unit