

US ATLAS Pixel Electronics

Issues to address:

- Overview of the ATLAS pixel electronics problem and ATLAS architecture
- Development process and institutional roles
- Schedule and Milestones
- Where are we ? A quick status report
- Basis of Estimate and Cost
- Summary

Basic Electronics Requirements

Geometry:

- Pixel size to be 50μ by $300\text{-}400\mu$, peripheral logic to be $\approx 2000\mu$

Overall Efficiency:

- Better than 95%, including deadtime, timewalk, dead channels, and geometry/overlaps. Individual contributions no more than about 1% each.

Timewalk:

- Less than ≈ 20 ns for “interesting” charges, $Q > Q_{\text{MIP}}/(3\text{-}5)$, where Q_{MIP} approaches 6 Ke after 10^{15} fluences

Input Threshold:

- Require ≈ 2 Ke with tolerable occupancy, and 2-4 Ke “in-time” threshold, with threshold dispersion less than $\approx 200e$

Noise and Noise Occupancy:

- Less than 200e noise, and less than 10^{-5} hits per crossing per pixel

Power Consumption

- Less than 40 μW /pixel front-end, and 250 mW/Front-end chip ($< 0.6 \text{ W/cm}^2$)

Leakage Current Compensation

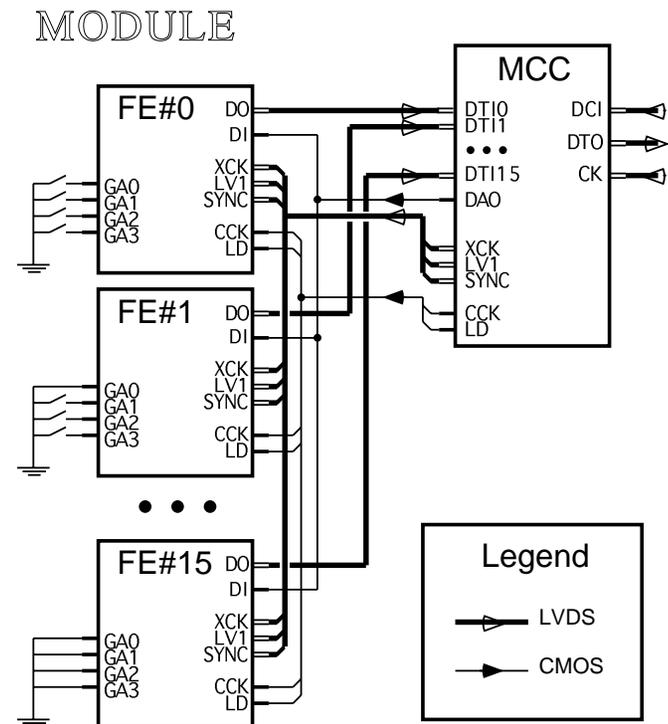
- Capable of sinking at least 50 nA without major operating point changes

Individual Pixel Calibration and Masking

ATLAS Baseline Configuration

Chip Functionality for Baseline Modules:

- Front-end chips will contain 24 columns of 160 pixels, plus 2 mm for peripheral logic, leading to a die size of 7.4 mm by 10.2 mm ($\approx 75 \text{ mm}^2$, limited by expected yields). Only sparsified data associated with L1 triggers is transmitted off-chip.
- MCC chips will service up to 16 FE chips in a star topology, using 40 MBit/s serial links
- Block diagram for demonstrator module electronics, showing basic interconnections between FE and MCC chips. Final interconnections and pinouts may be simpler.



Organization of Electronics Development Effort

Three major eras in design period:

- Parallel prototyping phase (“proof-of-principle”)
- Module “demonstrator” phase (realistic ATLAS prototypes)
- Pre-production phase

Now only two relevant rad-hard foundries. Pursue both:

- DMILL (0.8 μ 2-metal BiCMOS), and Honeywell (0.8 μ , 3-metal Bulk or SOI CMOS)

Prototyping phase:

- Three major lines of development (CERN/Genova, Bonn/CPPM, LBL)
- Follow initial concepts with goal of LHC “proof-of-principle”. Get experience with what works and what doesn’t

Demonstrator phase:

- Begin with ingredients and experience from prototyping phase
- Coordinate design activity to produce realistic prototypes to demonstrate operation of an ATLAS-like module (16 Front-end chips and a controller chip)

- Carry designs through for both rad-hard vendors, and test pre-/post-irradiation, leading to a vendor and final design choice

Demonstrator Activities:

- Specify chips to be built (FE-A is “DMILL” Front-end, FE-B is “Honeywell” Front-end, MCC is module controller chip)
- Build rad-soft ATLAS1 chips, 18 columns of 160 50μ x 400μ pixels, with all major functional blocks in an enlarged 3 mm periphery, including differential and serial I/O protocols. Geometry suitable for module construction (3 active sides, single row of pads on bottom).
- Build prototype ATLAS modules (16 FE chips, one MCC, realistic hybrids), and evaluate performance in detail.
- Build rad-hard ATLAS1 chips using two vendors. Evaluate complete modules pre- and post- irradiation.
- Build second-generation rad-hard ATLAS2 chips, 24 columns of 160 50μ x 300μ pixels, with complete peripheral logic in 2 mm space.

Pre-production phase:

- Make final changes in design, establish estimate of yield for production runs

What are Design Roles of Different Institutes ?

Bonn (no engineers, one physicist/designer, \approx 1 FTE):

- Plays significant role in characterizing all chips
- Leading system design and peripheral logic implementation for “DMILL” FE chip

CERN (two engineers, fraction of an FTE):

- Engineers participate in design discussions, but no formal role

CPPM (two engineers, 2 FTE):

- Major role in “DMILL” FE chip, including front-end and readout design

Genova (one physicist/designer, two engineers, \approx 2.5 FTE):

- Major role in overall system design, and lead role in MCC chip

NIKHEF (one engineer, \approx 0.5 FTE)

- Minor role in FE chips (I/O drivers), supporting role in MCC chip

What are US Roles in the FE Chip Design ?

Building “Honeywell” FE Chip

Front-end Design:

- Pursuing new solutions to several critical issues (timewalk, cross-talk rejection, threshold dispersion, and leakage current tolerance).
- Pursuing Honeywell front-end designs

Readout Architecture:

- Pursuing new, very low deadtime design, capable of implementation in either 2-metal or 3-metal processes but optimized for Honeywell

System Integration:

- Designing simple serial command decoder, digital bias control circuits, data serializer, and low-voltage differential drivers to build complete chip

Honeywell Characterization:

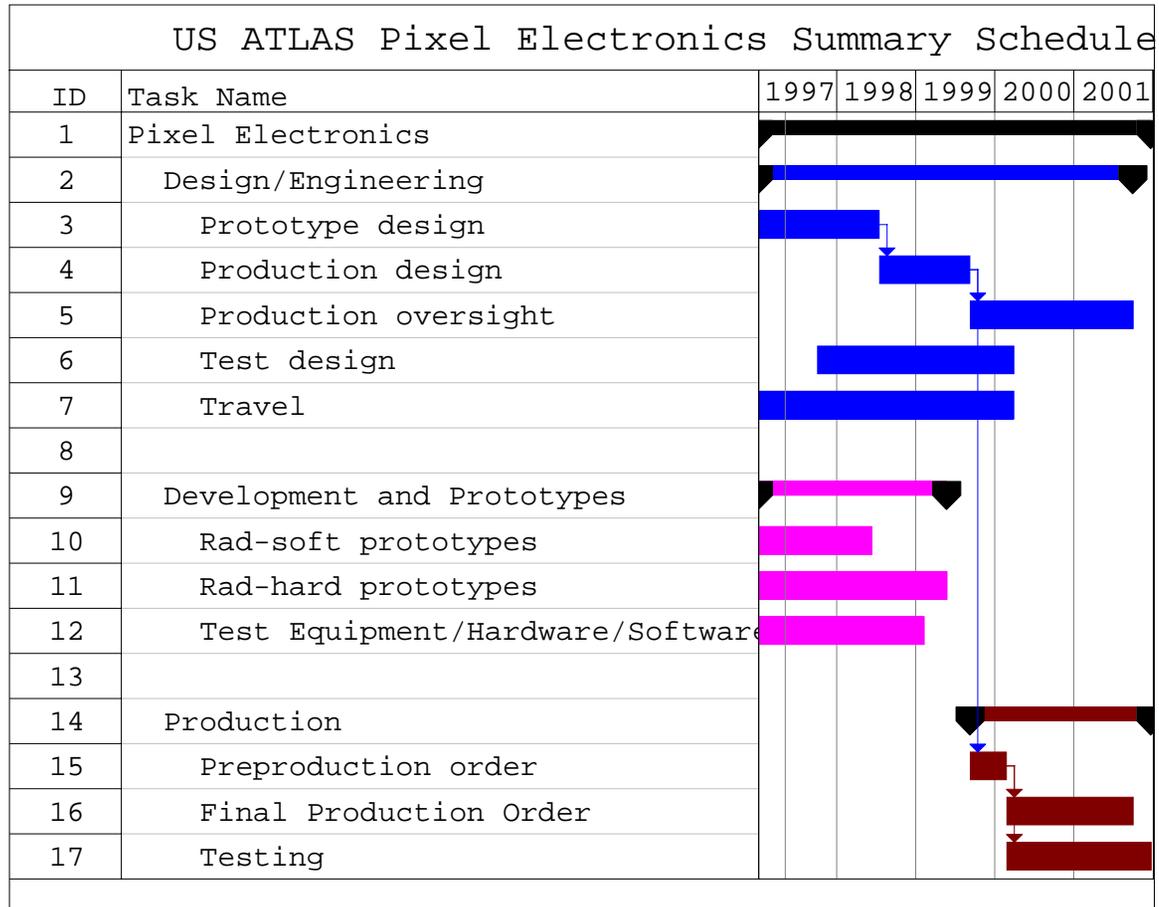
- Performance of Honeywell Bulk and SOI processes are poorly known for high doses (> 10 MRad). Collaborating with Honeywell, using their Process Monitors

Expect involvement at level of \approx 3-4 FTE of engineering throughout design phase

Pixel Electronics Milestones

- Mar 1996: Choose Analog vs Binary readout (choice is binary)
- Dec 1996: Terminate design efforts on “parallel prototyping” phase
- Apr 1998: Complete rad-soft demonstrator phase
- Dec 1998: Complete rad-hard demonstrator phase
- Aug 1999: Select rad-hard vendor (s)
- Sep 1999: Begin pre-production run
- Mar 2000: Release full electronics production
- Dec 2001: Complete full electronics production and wafer testing

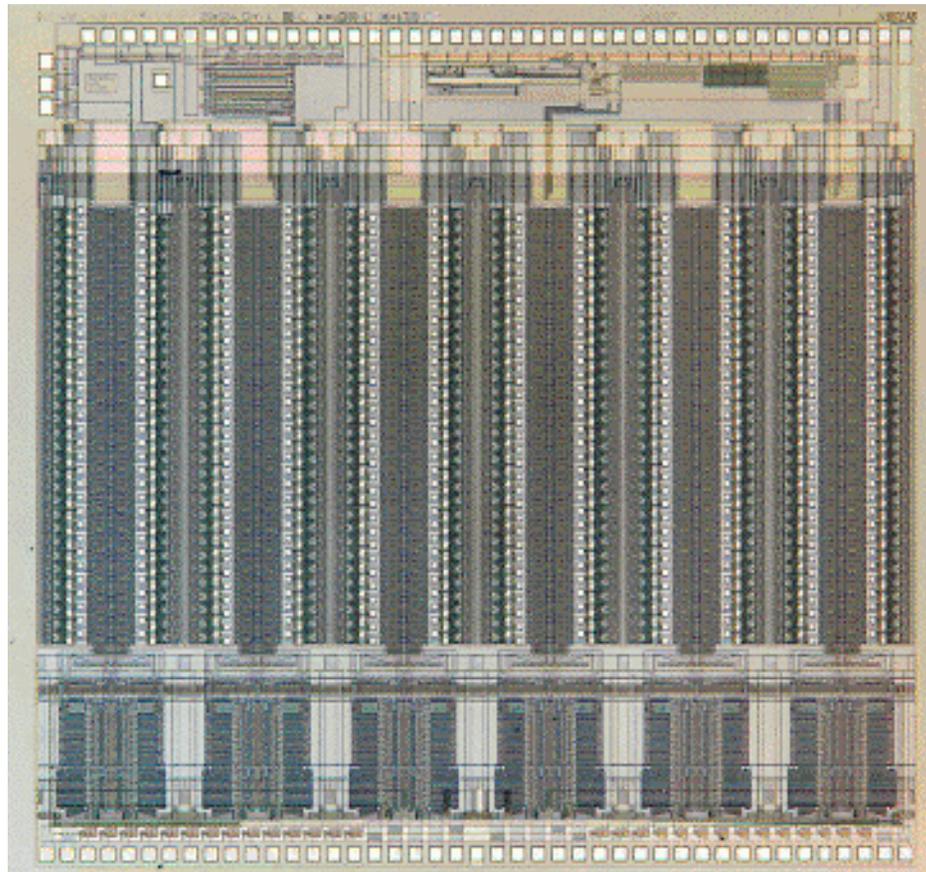
Pixel Electronics Schedule



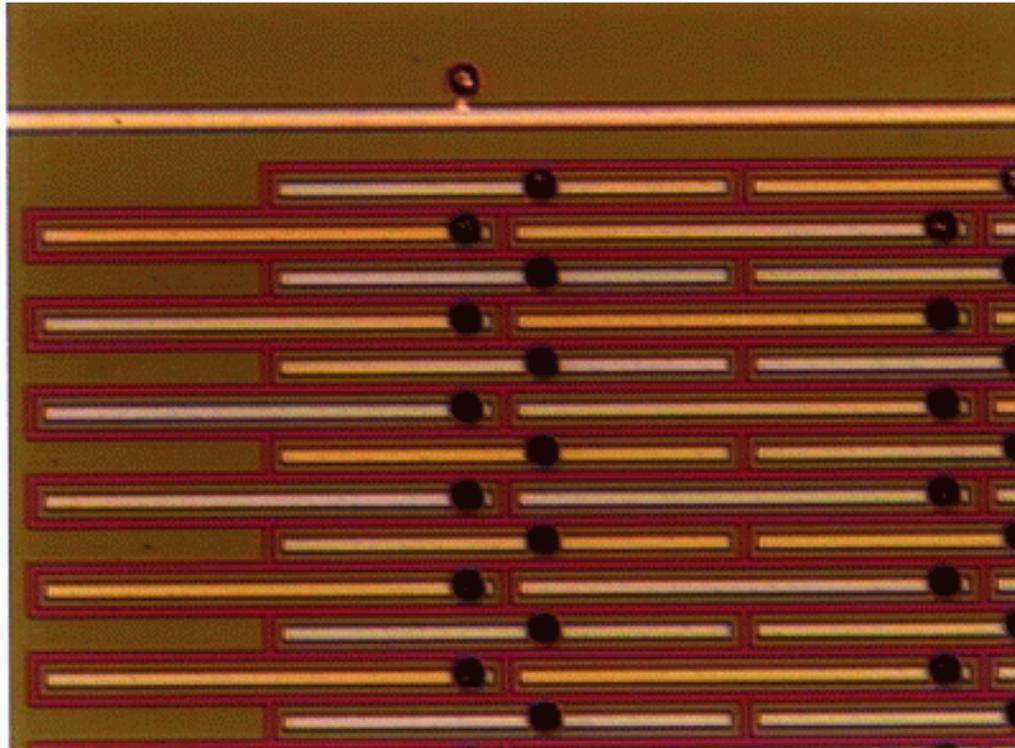
Status of US Effort

Prototyping Activities:

- Fabricated 12 column by 64 row array of $50\mu \times 536\mu$ pixels. It has negative polarity inputs, analog readout, and a complete functional prototype of LHC-capable peripheral logic, in the HP 0.8μ 3-metal process. Chips returned Jan 97, with two minor layout errors.



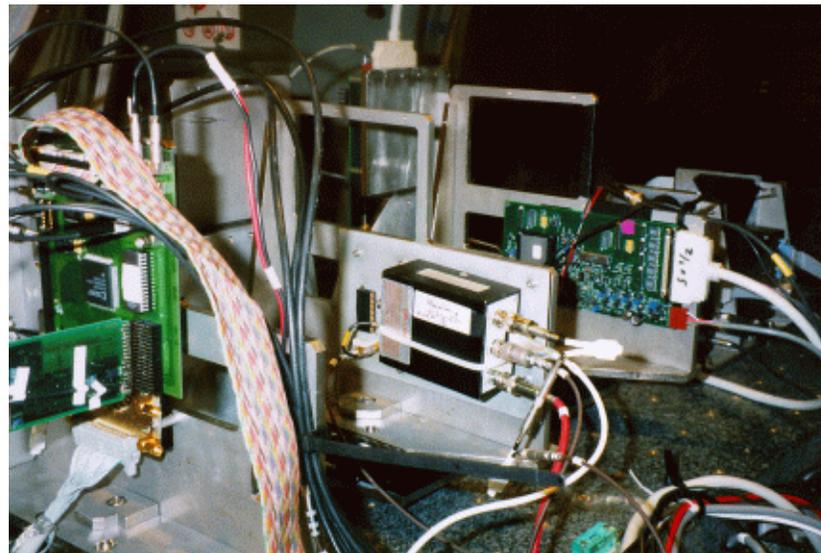
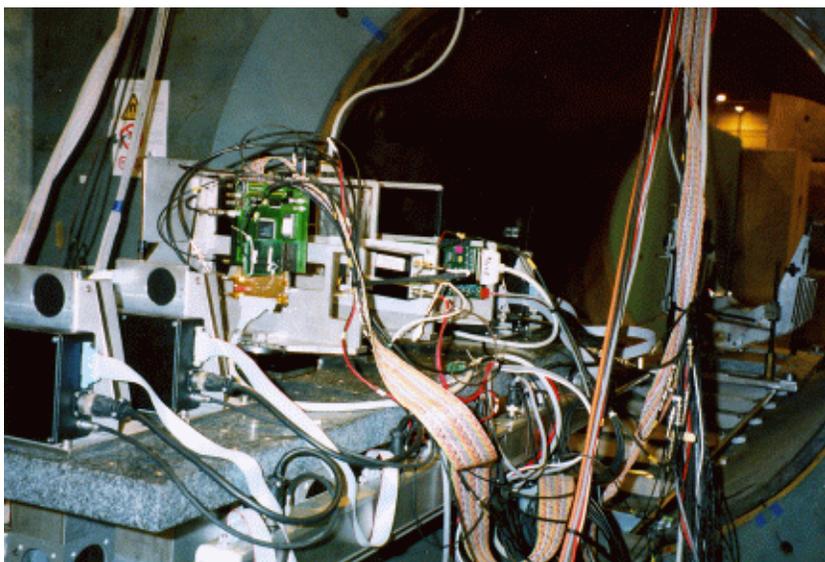
- Arrays were bump-bonded by Rockwell/Boeing, using 25μ Indium bumps, to bricked n-pixel on p-bulk detectors fabricated at LBL. Assemblies available at LBL in Mar. 97.



- Arrays with/without detectors were characterized using complete VME-based readout system to study threshold, charge measurement, and timing uniformity:
 - Threshold uniformity $< 200e$ (without) and $< 400-500e$ (with) detectors
 - Timing uniformity < 1 ns, but timewalk significantly worse with detectors (“in-time” threshold is acceptable for 50 ns, but not for 25 ns)
 - Charge measurement uniformity was relatively poor (\approx factor 2 variations)

H8 Test Beam Setup

Chip/detector assemblies in ATLAS test beam in Apr. 97:



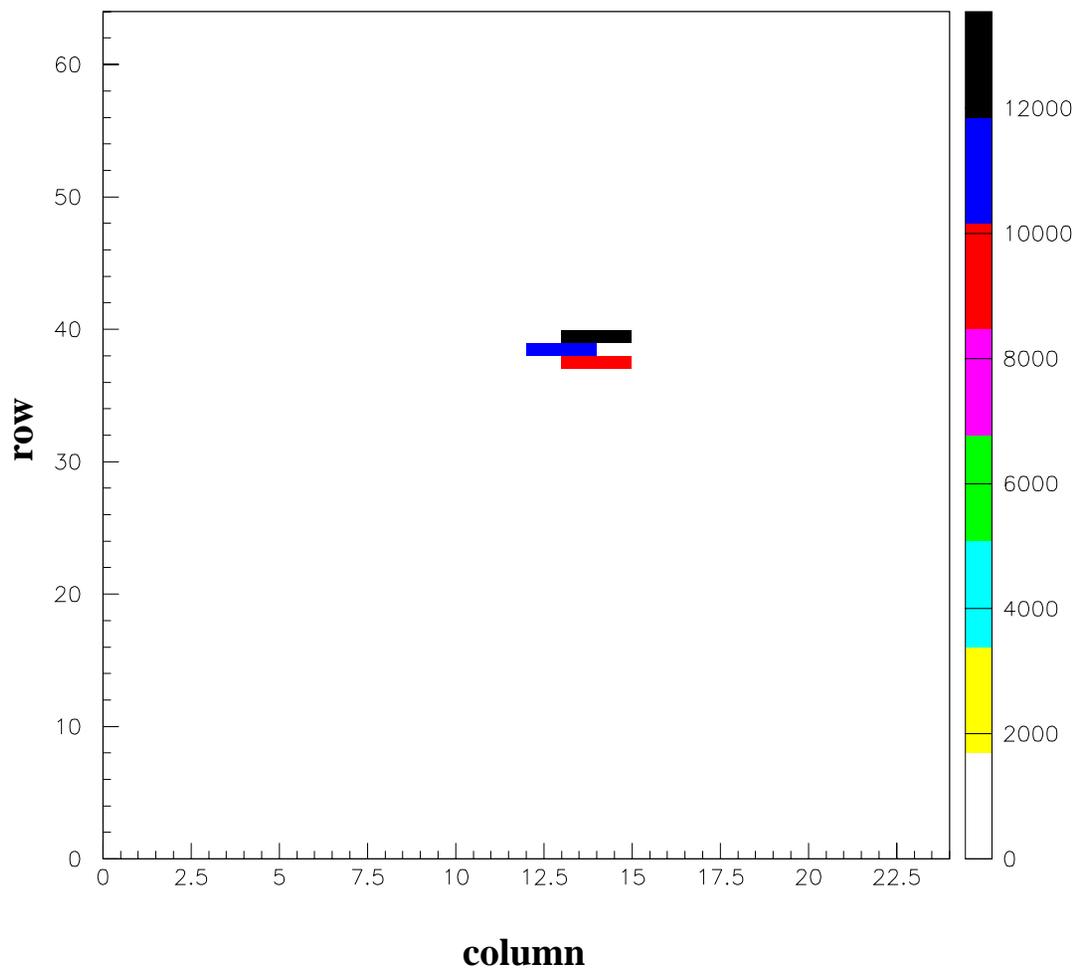
Test Beam setup in H8:

- Four pairs of 50μ strips in x-y planes with slow analog read-out (Viking), providing $1-2\mu$ point resolution
- Small silicon diode (5×5 mm) in trigger to select tracks in pixel arrays (3×6 mm)
- Superconducting dipole providing 1.5T vertical field
- Support stages with rotation/translation for Bonn/CPPM and LBL chips, which were operated simultaneously with common 40 MHz clock.

Preliminary Test Beam Results

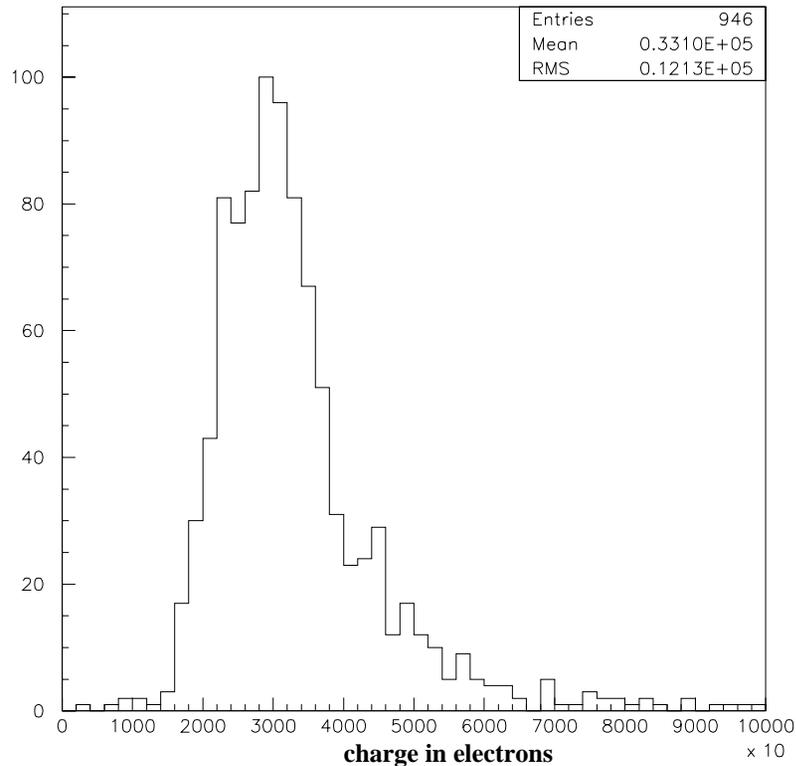
Chips operated with threshold of $\approx 4\text{Ke}$, and were very clean, with typically no extra pixels hit:

event display, $V = 50$, $B = \theta = 0$, $\Phi = 30$

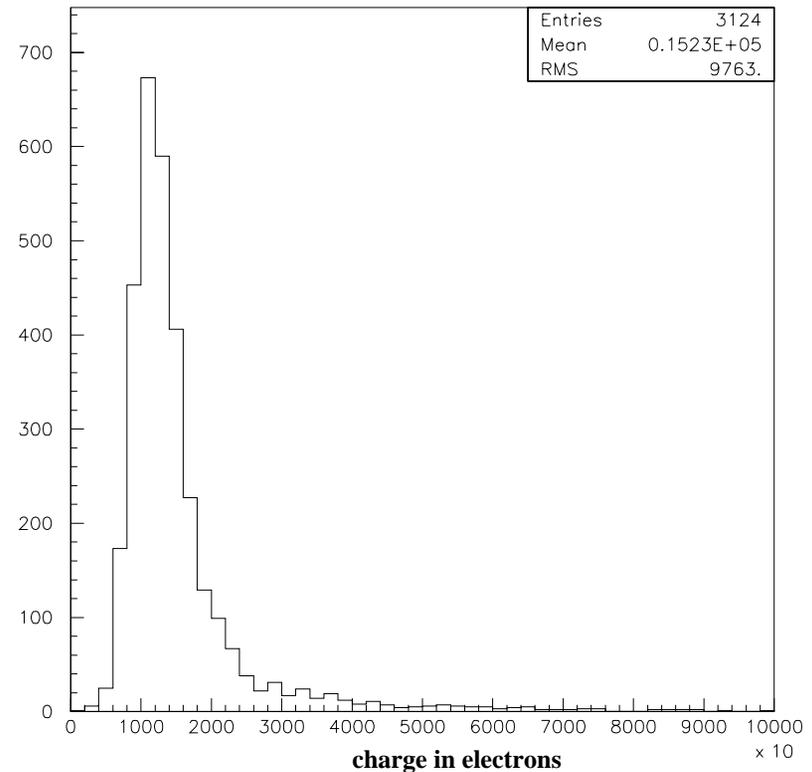


Due to charge measurement non-uniformities, apply per-pixel corrections, then plot charge distribution. Plots shown are for $\approx 250\mu$ depletion (50V) and $\approx 100\mu$ (10V) :

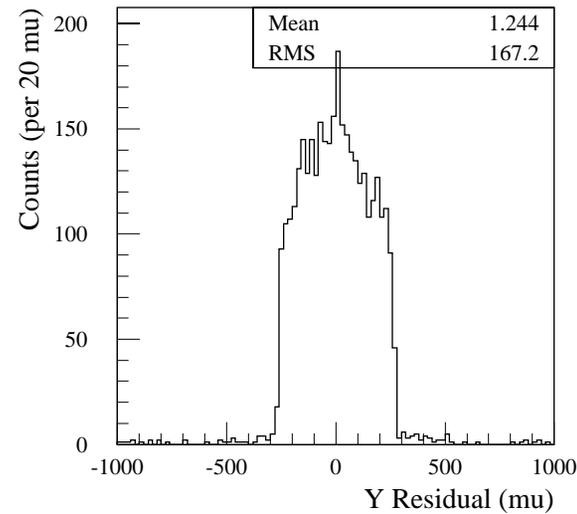
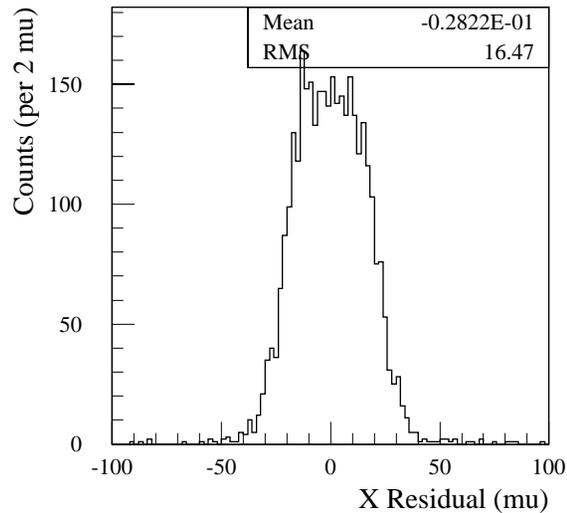
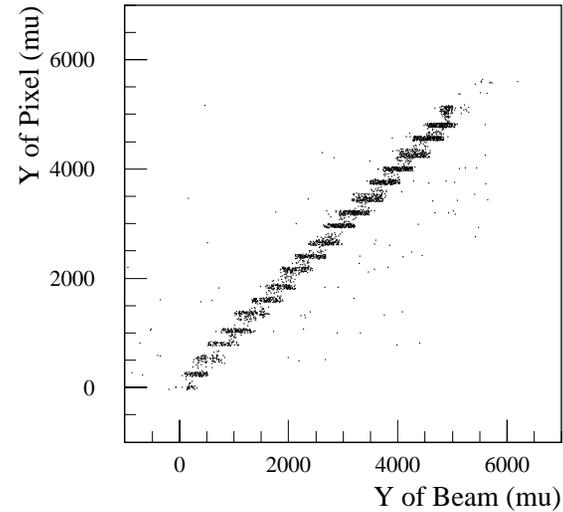
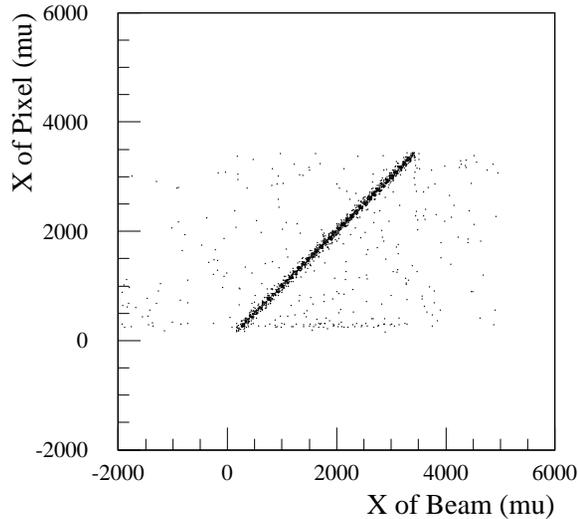
cluster charge distribution, 50 V, $B = \Phi = \theta = 0$



cluster charge distribution, 10 V, $B = \Phi = \theta = 0$



Using preliminary strip and pixel plane alignments, find hit matching efficiency > 95%, good correlations, with position resolutions roughly as expected (depletion $\approx 150\mu - 200\mu$):



Progress on Demonstrator FE-B Chip Design

Front-end Design:

- Have submitted three generations of prototypes for next-generation front-end design, including 3 MOSIS and one Honeywell submission.
- Now have essentially final design, and most recent submission will allow detailed characterization and final validation before making wafer-scale submission

Readout Architecture:

- Have submitted complete prototype of basic building block (column pair and its End-of-Column logic with concurrent input and output support).
- Remaining design issues will be addressed, prototype chip will be evaluated for possible optimizations or improvements.

System Integration:

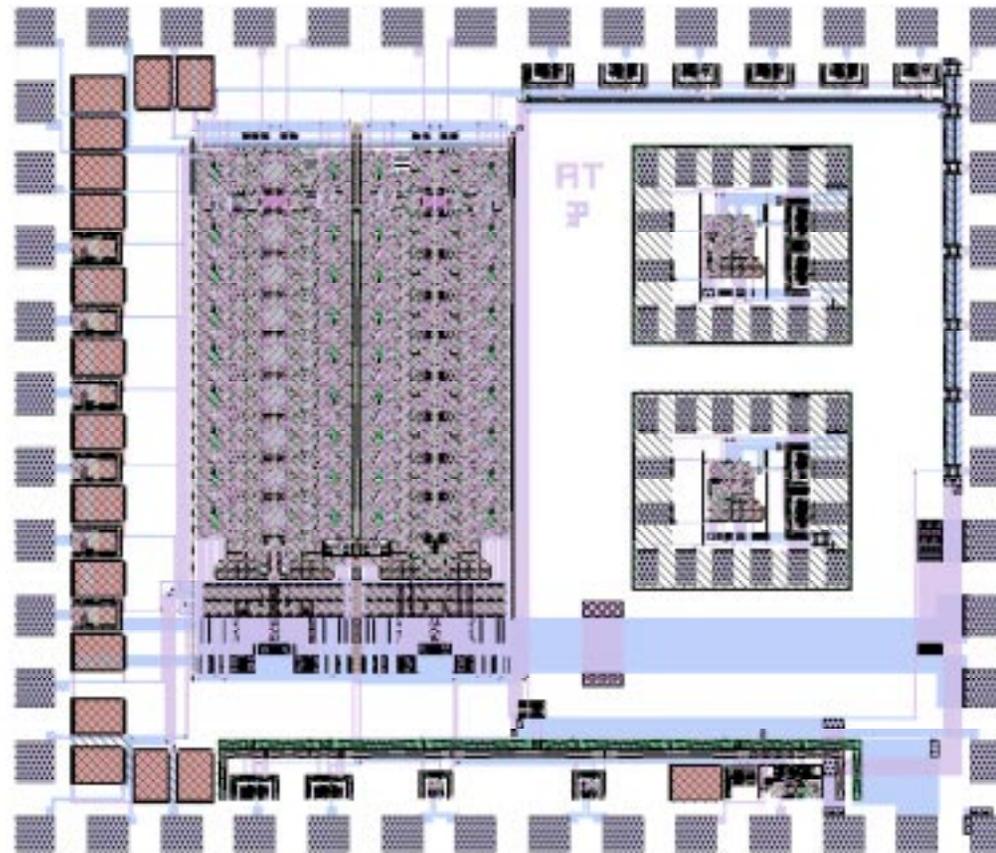
Design started on additional functional blocks, but schedule does not permit extensive prototyping (they are simple, but...)

Major issue will be integrating and verifying the complete chip: expect it to exceed the 1M transistor mark - a first for HEP ?

Prototype of new LBL Pixel Front-end Design

May 7 submission of next-generation front-end designs:

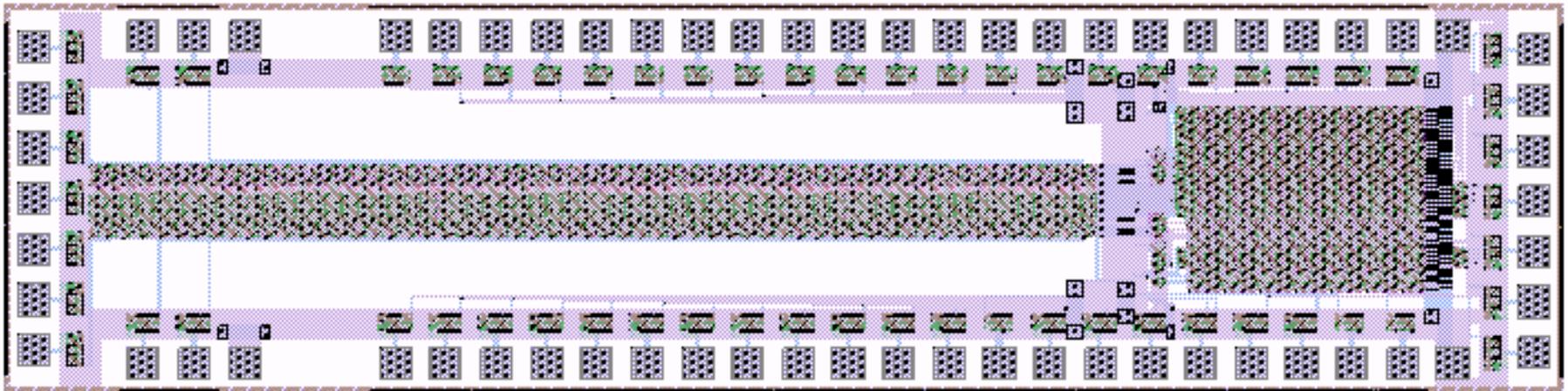
- Includes 2 column pairs (18 pixels per column) with real geometry, prototype pixel control logic (Select, Mask, Calibrate, and Tune circuits), and test options.
- Contains realistic biasing and vertical power bussing. Pixel size $\approx 130\text{-}140\mu$



Prototype of new LBL Digital Architecture

May 7 submission of column-pair prototype for new architecture:

- Transmits 7-bit Grey-code timestamp to each pixel, where leading/trailing edge timing is latched
- Data is asynchronously drained from pixels to periphery as soon as it is ready
- End-of-Column logic block contains 20 buffers, capable of storing hits from up to 16 different events. Trigger accept/reject operations all performed in EOC.
- Present size: pixel back-end is 120μ , and EOC buffer block is $\approx 600\mu$ by ≈ 1 mm



Basis of Estimate for US ATLAS Pixel Electronics

WBS 1.1.3.1 Design:

WBS 1.1.3.1.1 Prototype Design (design for ATLAS1 and ATLAS2 demonstrator chips)

- Design effort including senior and junior engineers, corresponding to ≈ 4 FTE during the two years when this activity peaks, making use of pieces of 3 senior and 3 junior engineers at LBL. A 25% contingency was assumed (equivalent to 6 months delay)

WBS 1.1.3.1.2 Production Design (design for pre-production follow-up to ATLAS2 chip)

- Most of the design is performed in the earlier phase. This phase assumes ≈ 3 FTE for the nine month period when this activity peaks. A 30% contingency is assumed (equivalent to a 3 month delay).

WBS 1.1.3.1.3 Production Oversight

- Estimated engineering required to “supervise” production, equivalent to $\approx 1/4$ FTE over 2 year production cycle.

WBS 1.1.3.1.4 Testing Design

- Estimated engineering for test board design and test procedure development. This is equivalent to $\approx 1/3$ FTE over the 3 year design period.

WBS 1.1.3.2 Chip procurement and test board fabrication:

WBS 1.1.3.2.1 Rad-soft prototypes

- This covers the “partial prototype” chips (front-ends only, digital readout only) for the original 12x64 array, plus the ATLAS1 array. It also includes the multi-project submissions for the complete 12x64 array, and the wafer-scale submission for ATLAS1.

WBS 1.1.3.2.2 Rad-hard prototypes

- This includes a single multi-project submission we made to Honeywell, plus the US share of the common procurement for the ATLAS1 and ATLAS2 rad-hard wafer-scale runs.

WBS 1.1.3.2.3 Test equipment

- This includes test cards, wafer probe cards, and miscellaneous hardware and software

WBS 1.1.3.3 Production:

WBS 1.1.3.3.1 Pre-production order

- This covers the US share of the common procurement cost for a pre-production order of 20 wafers from a single vendor.

WBS 1.1.3.3.2 Production order

- This covers the US share of the common procurement of the production run (US share fixed to be 275 6" wafers). The wafer count assumes realistic die leverages, a $\approx 30\%$ yield, and a 30% assembly loss. The cost is estimated from a TEMIC/DMILL quote for a 1000 wafer production run in 1999. The contingency is estimated to be 35%, using a Honeywell quote, and adding additional yield and assembly losses.

WBS 1.1.3.3.3 Testing

- We assume that the US wafers will be tested at LBL on an existing probe station, and estimate a probing rate of ≈ 2 wafers/day based on recent experience with SVX chips at LBL. This item includes equipment and labor.

Summary

US ATLAS Pixel Electronics is making significant progress:

First results from pixel arrays in test beam:

- Operation at 40 MHz, satisfying many ATLAS requirements, has been demonstrated.
- Many goals of the initial LHC “proof-of-principle” prototype program have been achieved

Significant submissions in next-generation design program:

- Realistic front-end prototype and new readout architecture prototype submitted
- Good indications that complete array submission can occur in late summer, providing the first realistic ATLAS prototype chips

Design well-enough defined to provide first reliable cost and schedule information - should be able to write TDR in April 1998.

US Role is well-defined and very significant - our intellectual and design contributions outweigh our construction responsibilities.